

Design of Decoder Using Domino Logic Circuit for VLSI

K. Rama Krishna Reddy^{1,*}, Sai Teja Ankuru², Divya Pillutla², Varthya Shirisha²

Abstract

Dissipation of power from a circuit is the major issue in the design of any VLSI circuit, which decreases the life span of a device/system. NMOS and PMOS circuits are very slow while switching the state from low to high. The speed of the circuit can be increased by decreasing resistance. This process in turn increases the static power dissipation. So, because of these disadvantages, CMOS circuits are used in many applications. For any CMOS circuit, the dissipation of power can be both static and dynamic. Dynamic dissipation in CMOS circuits occurs because of the switching of states. However, the static power dissipation is negligible in the circuit. Circuits designed using the domino model are used in various applications, like full adders, multiplexers, in memory as address selectors, comparators, and arithmetic circuits. There are different issues in domino logic circuits, namely power consumption, speed, and power delay product. A model is designed based on various approaches to solve these issues.

Keywords: Domino Logic Circuit, High speed, Low power

INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) is used for a large number of applications in the VLSI. It has become an important choice in the design of many logic circuits because its power dissipated from the circuit is very less and also it can be designed easily. It is the main advantage of CMOS logic over the other approaches and it has a problem with the leakage current flow and the dissipation of currents. The rapid growth in VLSI technology made the characteristics like high speed, less power, increased efficiency, and less area are main requirements of a circuit.

The speed of operation and area of the circuit became the priority of choice for the fabrication that led to the invention of Dynamic logic, and Domino logic families use the clock for synchronization. Power dissipation, speed, fabrication cost, and area are the key parameters to consider while designing any digital logic circuit. There may also need other requirements to meet in the application of design. The implementation should perform by considering all of these parameters into account [1–4].

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Because of its high speed and less cross-sectional area because of the smaller number of transistors, domino logic is chosen to design various digital circuits. With the advancement in many design technologies, the need to improve the available models or develop new models to achieve the multiple requirements to eliminate the drawbacks regarding existing models.

The number of transistors accommodated on the chip is increasing, and the size of the chip is decreasing in modern VLSI technology is the primary reason behind the scaling. After the evolution of the CMOS logic circuit, the scientist implemented static and dynamic logic circuits.

Dynamic logic circuits use widely because of their advantages as low delay, low power consumption, and smaller area are required compared to static logic circuits. Domino logic circuit is a type of dynamic logic circuit [5]. It uses in circuits where high performance is the primary factor. Domino logic circuits use a smaller number of transistors. The primary goal of the VLSI domain is to increase the number of transistors accommodated on the chip but to reduce the size of the chip. The size of the chip can reduce in three ways:

(1) By using advanced technology like scaling. (2) By circuit modelling techniques. (3) By careful chip layouts.

Figure 1 depicts the design of the Basic Domino logic circuit, which contains a dynamic logic circuit along with an additional NOT gate (inverter). The pre-charge phase and the evaluation phase are two phases of Domino logic. The output of the capacitor gets charged during the pre-charge phase only [6]. However, the result is correct only in the evaluation phase where the clock signal shifts from high logic level to low logic level. The logic gates such as AND, OR, and inverter are choosing to get the non-inverting output implementations at the domino logic level. But logic gates such as NAND, NOR, and Inverters ain't be used. Throughout many designs, inverting functions are unavoidable, which appears to prohibit the wide use of domino logic at first glance. Moreover, because of evaluation node is recharged in domino logic cells, the clock signal shifts from a low level to a high level are considerable, which is in general unacceptable [7].

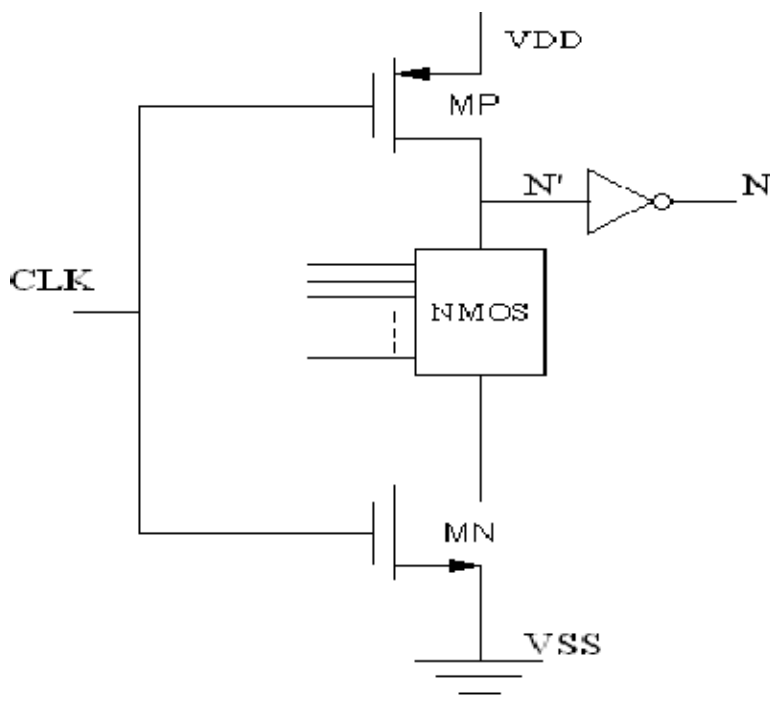


Figure 1. Domino Logic circuit.

Signal nodes in a static model toggle multiple times before achieving a final steady-state, whereas they are missing in domino architecture. Because if the output of the cell increases, unchanged in the cell's input causes the result to fall. Only when the clock strikes zero at the end of the assessment period will the cell's output decline. As a result, one rise and fall at the domino cell's output is possible throughout a clock period [8]. Charge redistribution and noise margin issues exist within parasitic capacitances at the circuit's nodes, resulting in misleading output. Domino logic has a single clock that recharges the dynamic node of the domino during the pre-charge phase and assesses the function in the evaluation stage performed by the NMOS network.

DESIGN OF DOMINO LOGIC CIRCUIT FOR 2-INPUT OR LOGIC

In the article, below two types of domino logic models are implemented. They are the Basic Domino Logic circuit and Proposed domino logic circuit model.

The evaluation network should be a parallel connection of NMOS transistors to design an OR gate. In Figure 2, the Basic Domino Logic circuit, the clock signal shifting between high to low charges the capacitor at the dynamic node during the pre-charging phase [9]. The combination of inputs for the evaluation network does not influence the output. While at the evaluation phase, the clock shifts from low logic to high logic. The capacitor at the dynamic node discharges through the evaluation network depending on the combination of inputs. The inverter output is the required output for input combinations.

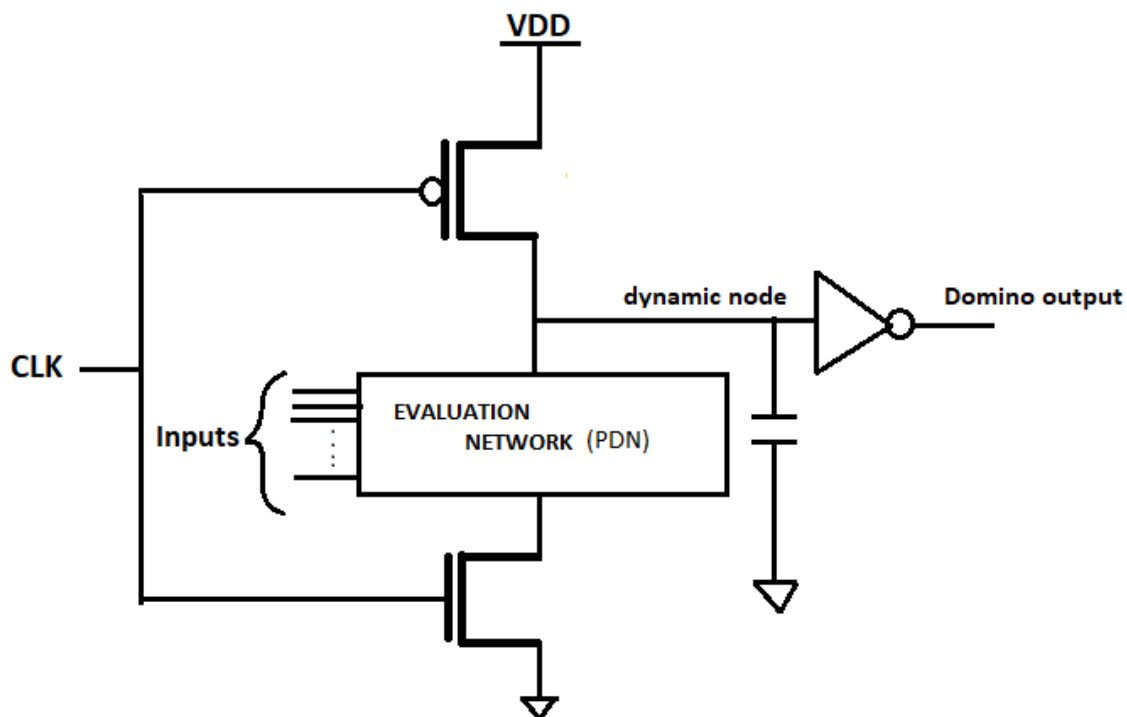


Figure 2. Basic Domino Logic Circuit.

In Figure 3, the proposed domino logic circuit comprises of enable signal that should be enabled throughout all times to get static output even during the pre-charge period. The proposed domino logic circuit works in the following way: If the clock signal is at a low level (generally termed the charging phase), the MN1 transistor turns off. The capacitor at the dynamic point either charges to supply voltage VSS or discharges to the ground, depending on the combination of input logic at the evaluation network. If inputs make the dynamic node drain to the footer voltage, then energy uses a level restorer to discharge and can also supply correct outputs regardless of the input by a clock [10]. The circuit has an enable input that is used explicitly. As a result, if no input discharges the dynamic node, the ground level is raised to the keeper circuit, and multiple shifts are permitted in all instances.

IMPLEMENTATION OF DESIGN

The design of both the Basic Domino Logic model for AND gate and the Proposed Domino Logic model for AND gate is implemented in an application i.e., a 3x8 Decoder circuit depicted in Figure 4. In general, a decoder circuit provides the necessary output as soon as the input combination arrives. However, in large circuits/networks, if the decoder circuit has an isolated period, then there is no change in the output even though for a change in the input combination [11]. In the remote time, if the clock input in the circuit is in the pre-charge phase, then the clock is disabled, restricting the decoder

from changing the output. However, when the evaluation phase starts, enabling the clock signal to shift from logic low to logic high makes the decoder shift the result to the input combination available [12].

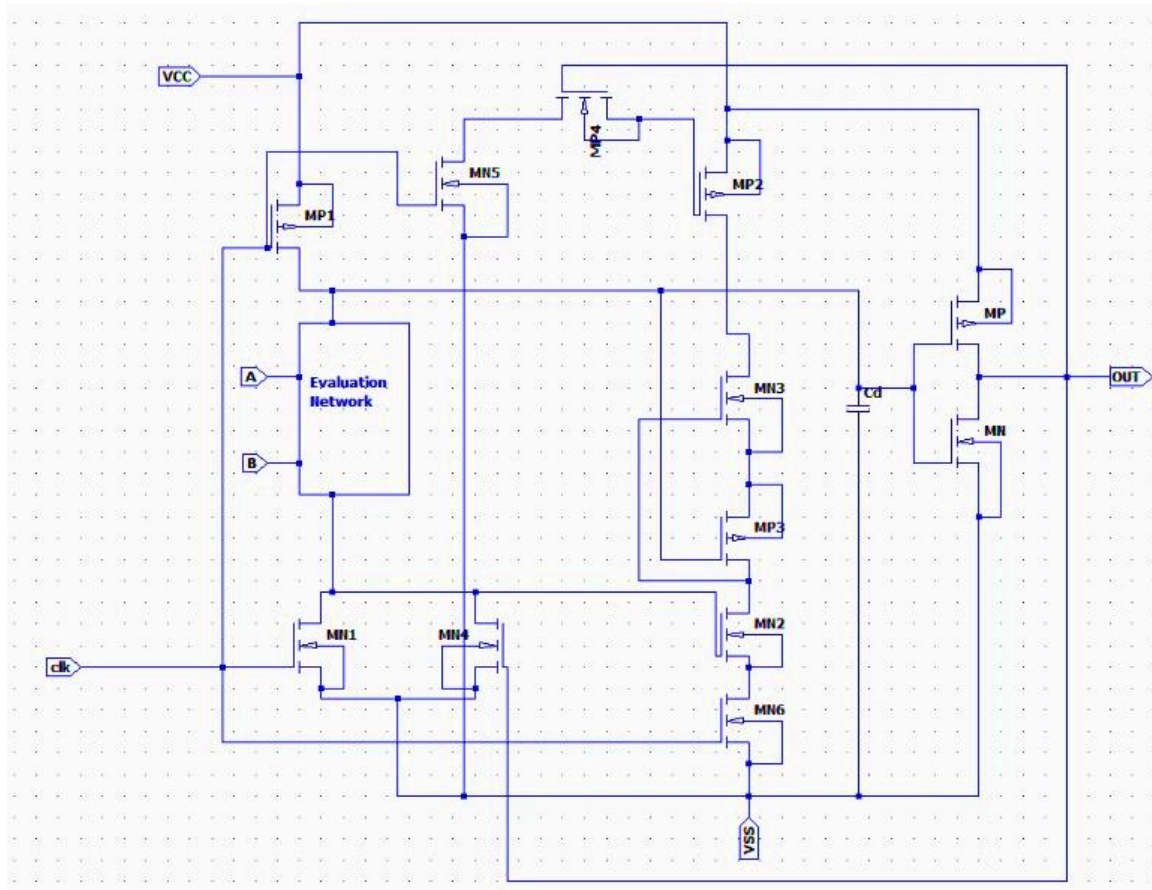


Figure 3. Proposed Domino Logic Circuit.

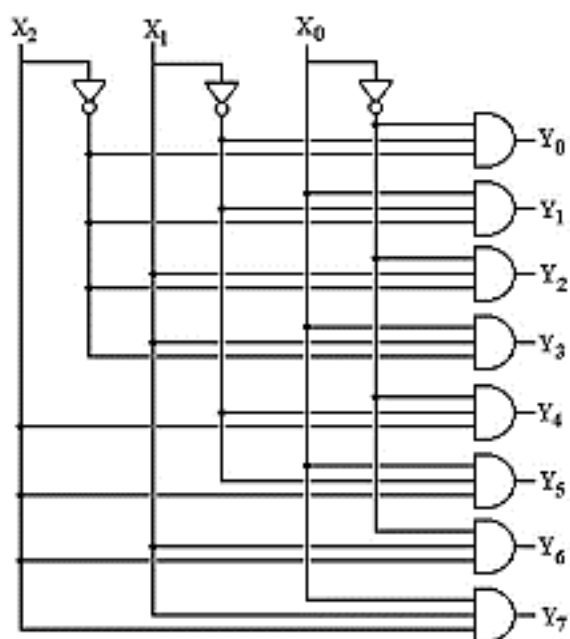


Figure 4. 3x8 Decoder.

SIMULATION RESULTS

Figure 5 depicts the design of a Basic Domino Logic circuit for an AND gate using the LT Spice software tool by 180nm technology, with voltage supply $V_{SS} = 1.8\text{V}$ and a clock frequency = 500 MHz.

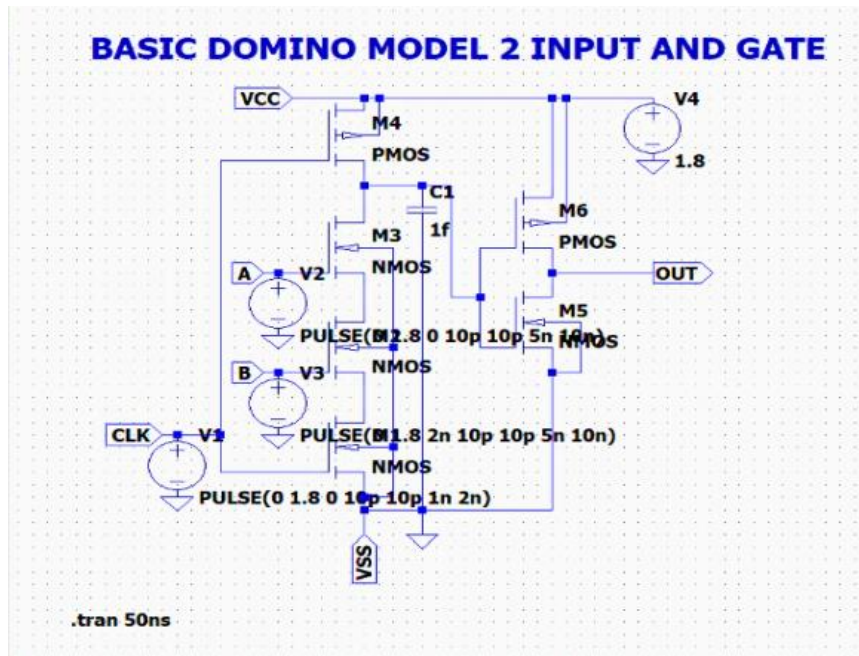


Figure 5. Basic Domino Logic of AND Gate.

The simulations of Basic Domino Logic of AND gate and graphical representations are compared with the AND gate's truth Table in Figure 6.

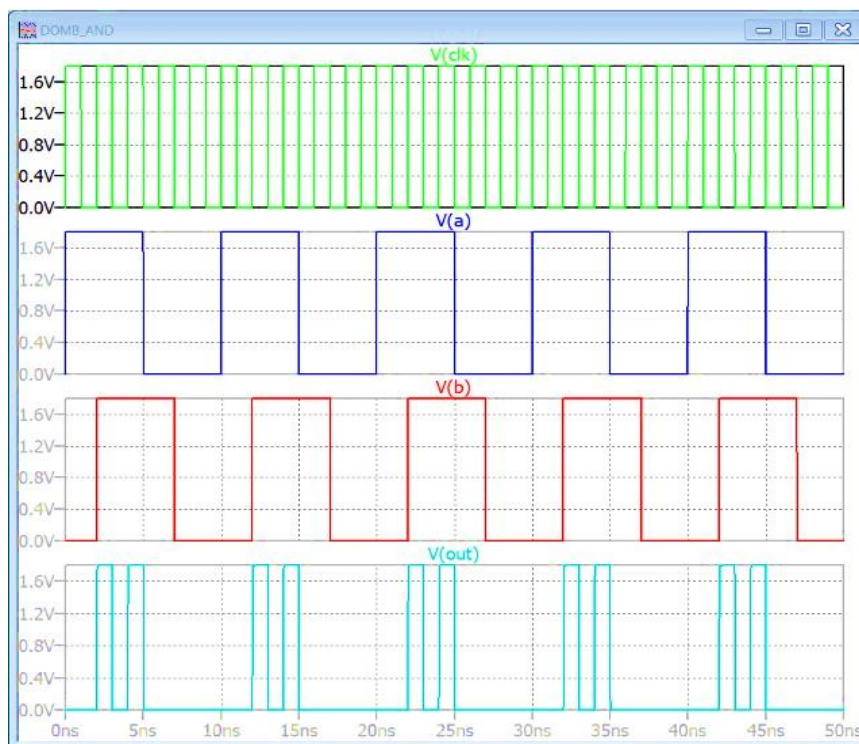


Figure 6. Graphical representation of Basic Domino Logic AND Gate.

Figure 7 depicts the model of a Proposed Logic circuit of an AND gate using the LT Spice software tool by 180nm technology, with voltage supply VSS = 1.8v and a clock frequency = 500 MHz.

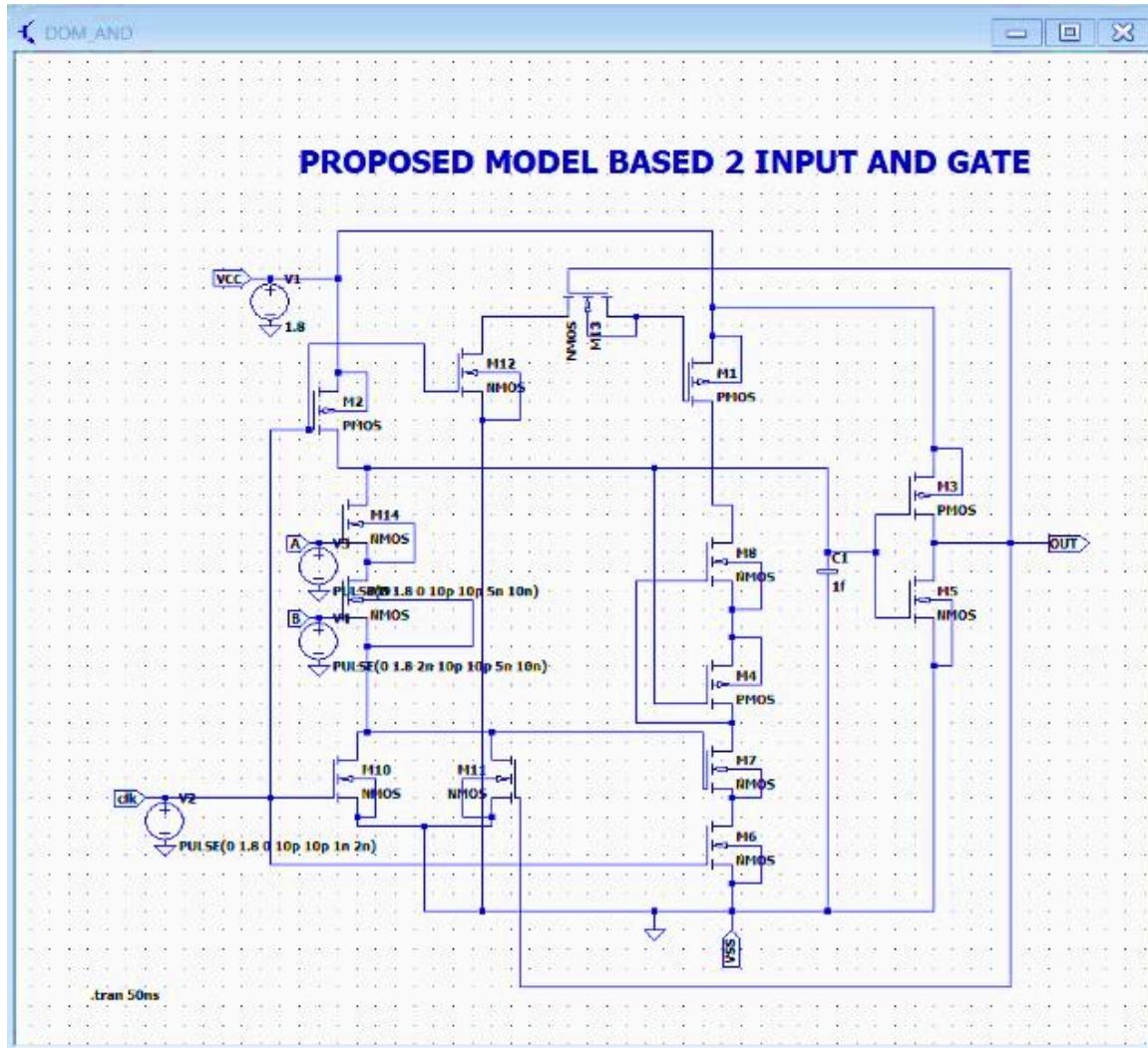


Figure 7. Proposed Domino Logic of AND Gate.

The simulations of the Proposed Logic for an AND gate and the graphical representations are compared with the AND gate truth table in Figure 8.

Figure 9 depicts the model of a Basic Domino Logic circuit of an OR gate using the LT Spice software tool by 180nm technology, with voltage supply VSS = 1.8v and a clock frequency = 500 MHz.

The simulations of the Basic Domino Logic of an OR gate and graphical representations are compared with the truth table of the OR gate in Figure 10.

Figure 11 depicts the model of a Proposed Logic of an OR gate using the LT Spice software tool by 180nm technology, with a voltage supply VSS = 1.8v and a clock frequency = 500 MHz.

The simulations of the Proposed Logic of an OR gate and graphical representations are compared with the truth table of the OR gate in Figure 12.

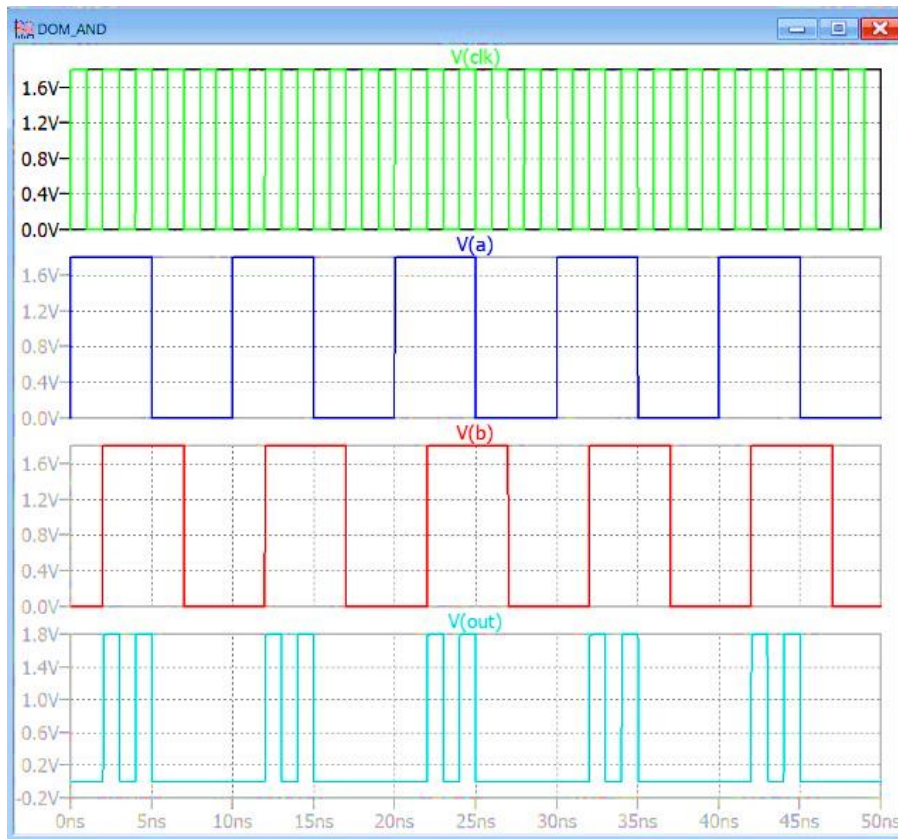


Figure 8. Graphical representation of Proposed Domino Logic of AND Gate.

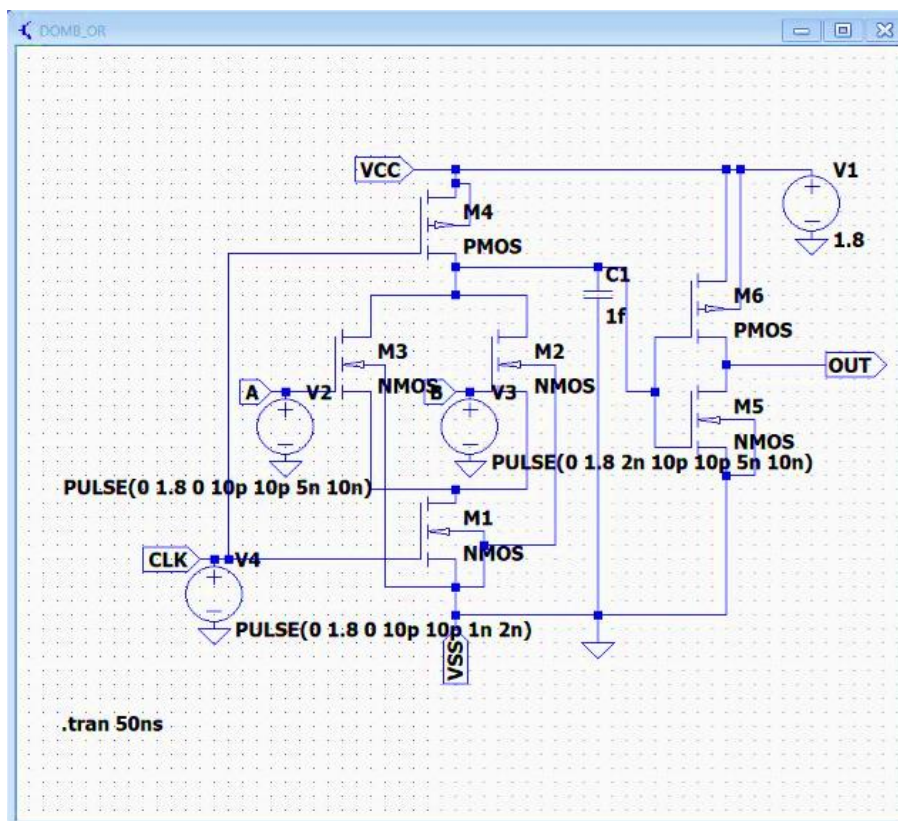


Figure 9. Basic Domino Logic of OR Gate.

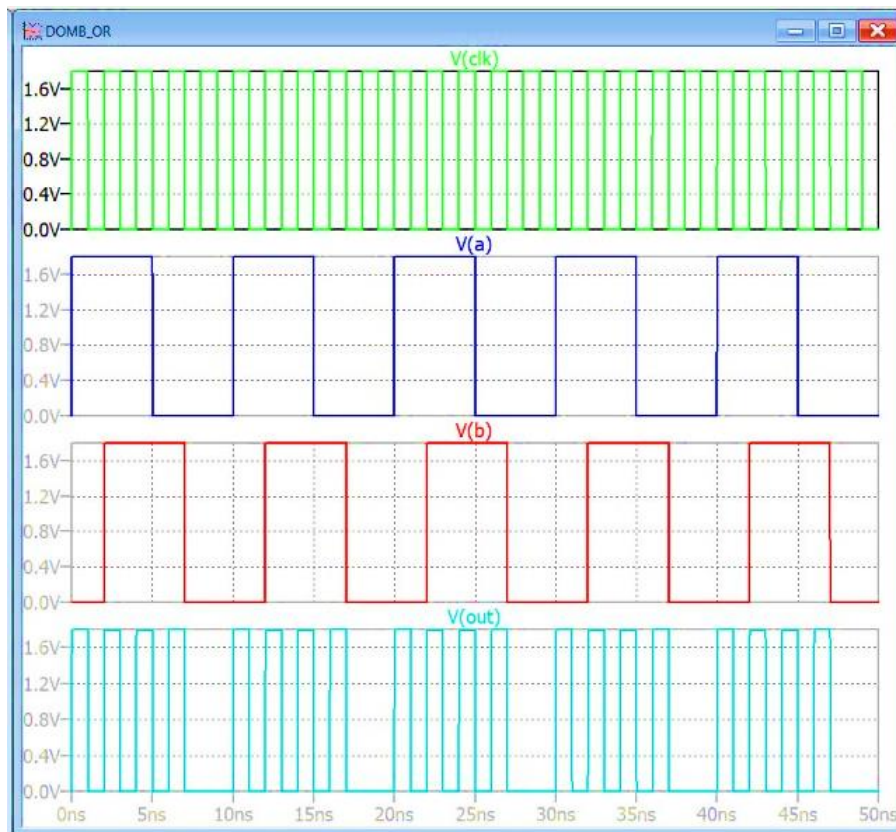


Figure 10. Graphical representation of Basic Domino Logic of OR Gate.

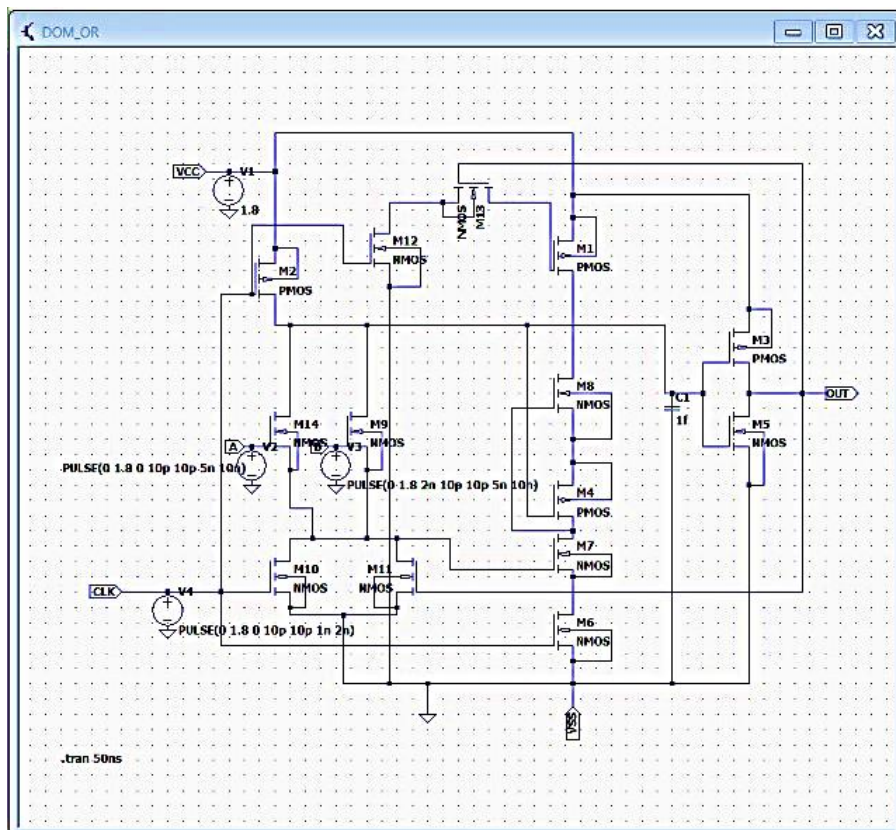


Figure 11. Proposed Domino Logic of OR Gate.

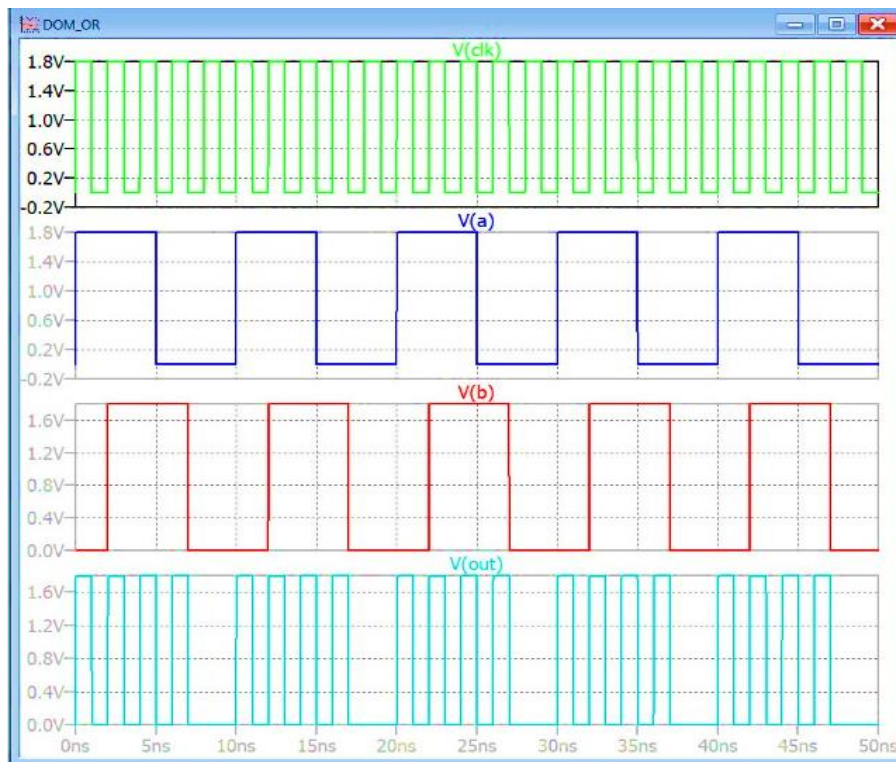


Figure 12. Graphical representation of Basic Domino Logic of OR Gate.

Figure 13 depicts the model of a Basic Domino Logic circuit for a 3x8 Decoder gate using the LT Spice software tool by 180nm technology, with a voltage supply $V_{SS} = 1.8\text{v}$ and a clock frequency = 500 MHz.

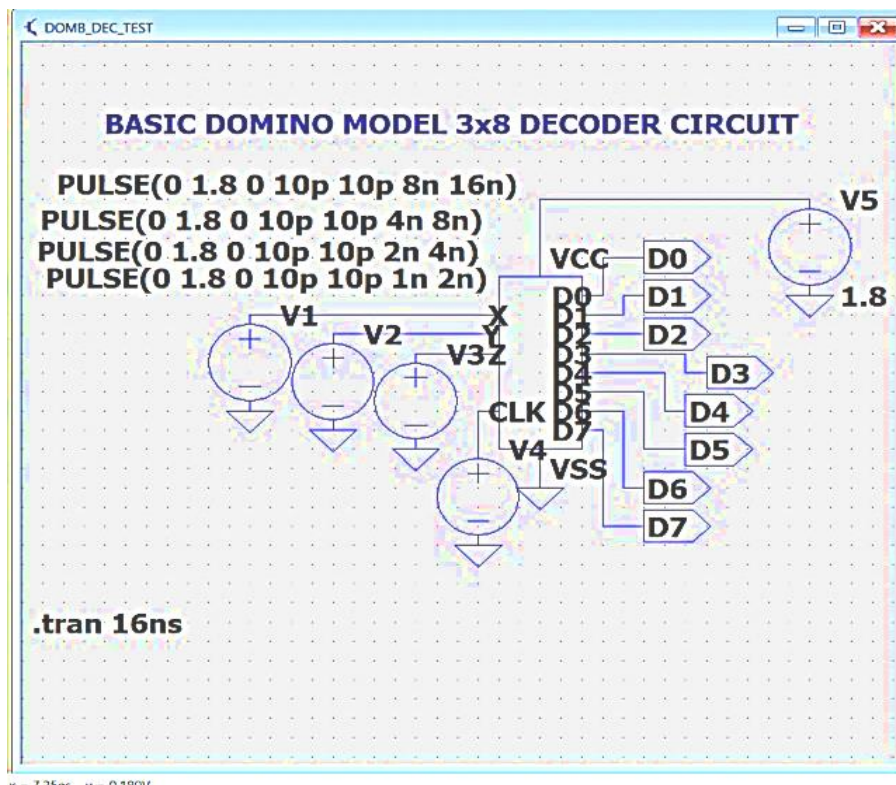


Figure 13. Basic Domino Logic of 3x8 Decoder.

The simulations of Basic Domino Logic of a 3x8 Decoder circuit and graphical representations are compared with the truth table of the 3x8 Decoder in Figure 14.

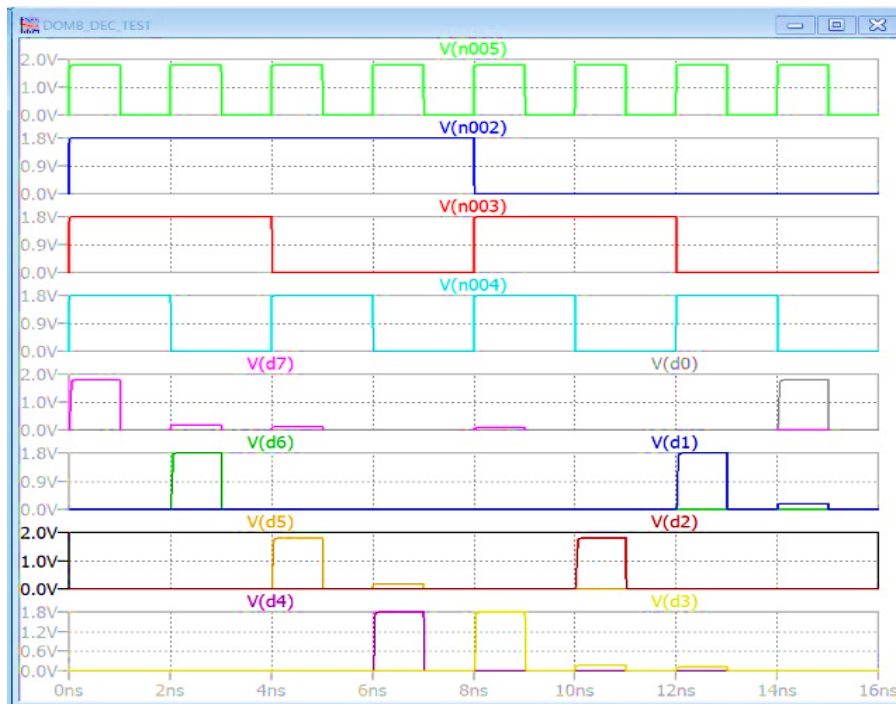


Figure 14. Graphical representation of Basic Domino Logic of 3x8 Decoder.

Figure 15 depicts the model of a Proposed Logic of a 3x8 Decoder using the LT Spice software tool by 180nm technology, with a voltage supply $V_{SS} = 1.8\text{v}$ and a clock frequency = 500 MHz.

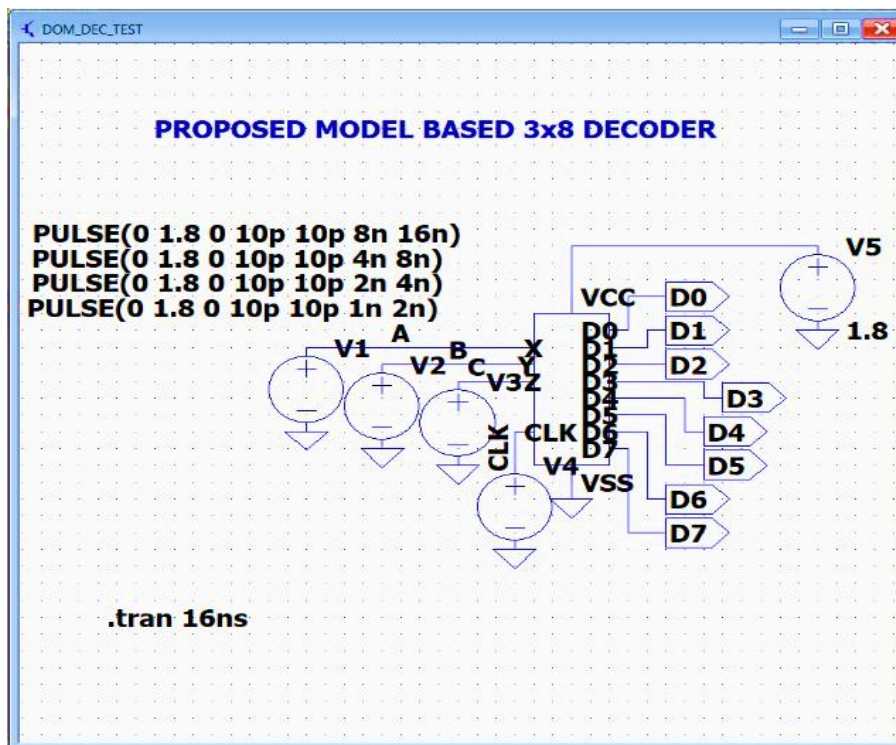


Figure 15. Proposed Domino Logic of 3x8 Decoder.

The simulations of the Proposed Logic for the 3x8 Decoder circuit and graphical representations are compared with the truth table of the 3x8 Decoder in Figure 16.

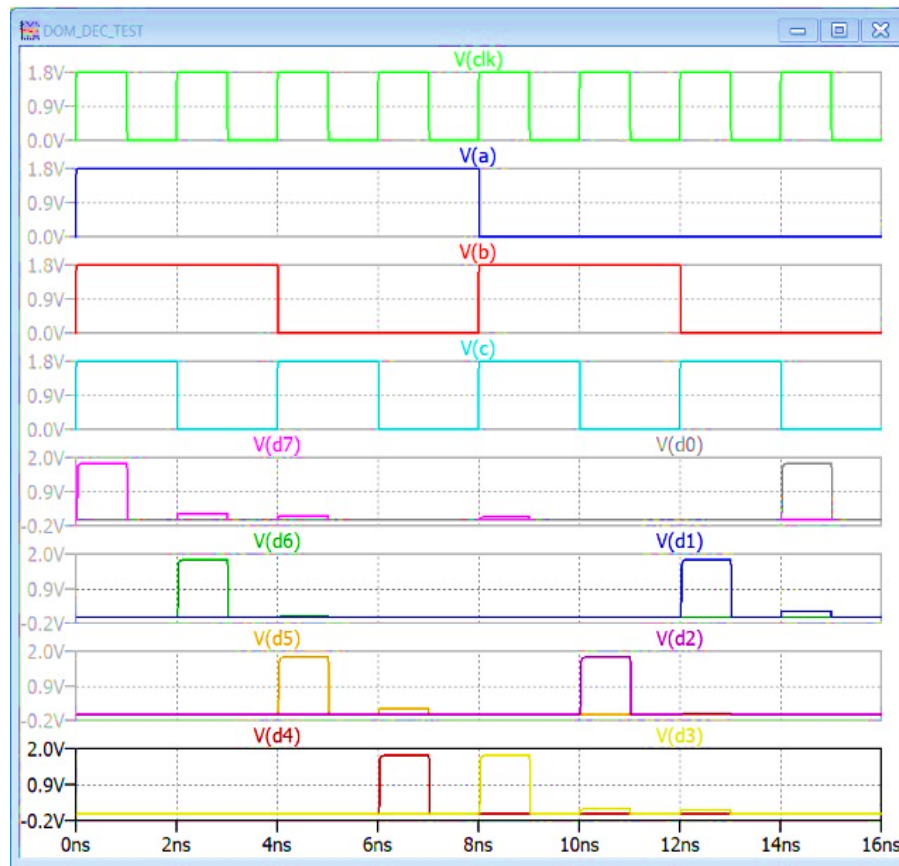


Figure 16. Graphical representation of Proposed Domino Logic 3x8 Decoder.

Table 1 compares the dissipated power, delay of propagation, and power-delay product testing results of both logic models for a 2-input AND gate. Table 1 shows, that the proposed logic for AND gate has less power, delay, and power delay product than the basic domino logic circuit.

Table 1. Comparison values of Power dissipation, Delay, and PDP for first logic model.

Domino logic Circuits	Power Dissipation (μW)	Propagation Delay(ps)	PDP (aJoule)	Area
Basic Domino Logic Circuit	1.21	15.51	18.73	6
Proposed Domino Logic Circuit	1.06	14.70	15.69	14

Table 2 compares the dissipated power, delay of propagation, and power-delay product testing results for both logic models for a 2-input OR gate [13–15]. Table 2 shows, that the proposed logic for the OR gate has less power, delay, and power delay product than the basic domino logic circuit.

Table 2. Comparison values of Power dissipation, Delay, and PDP for second logic model.

Domino logic Circuits	Power Dissipation(μW)	Propagation Delay(ps)	PDP (aJoule)	Area
Basic Domino Logic Circuit	2.18	8.56	18.66	6
Proposed Domino Logic Circuit	2.04	7.39	15.13	14

Table 3 compares the dissipated power, delay of propagation, and power-delay product testing results for both the logic models for the 3x8 DECODER circuit. Table 3 shows that the proposed logic for the 3x8 DECODER circuit has less delay and power delay product than the basic domino logic circuit.

Table 3. Comparison values of Power dissipation, Delay, and PDP for decoder circuit.

Domino logic Circuits	Power Dissipation (μ W)	Propagation Delay (ps)	PDP (aJoule)	Area
Basic Domino Logic Circuit	28.60	29.41	841.44	54
Proposed Domino Logic Circuit	29.28	28.50	834.66	118

CONCLUSION

This paper gives a thorough introduction to dynamic logic and its shortcomings, as well as domino logic circuits, their properties, and the advantages of domino logic circuits. The power dissipated and the speed of the circuit has been compared with the basic domino model and proposed domino model. The basic domino logic circuit and the proposed domino logic circuits have been reviewed in the literature. The two-threshold domino logic circuit lowered leakage current, lowering the circuit's overall power dissipation. In the article, both the basic logic, and the proposed logic for OR logic gate, AND logic gate, and 3x8 Decoder are designed using 180nm technology, with a supply voltage $V_{SS} = 1.8V$, and clock frequency = 500MHz in the LT Spice software.

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