

Comparative Analysis of CMOS CNFET and Memristor Based Full Adder Circuits and CMOS Memristor Based Multiplexer Circuits

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Abstract

Continued developments in microelectronics technology have led to a myriad of new compute-intensive applications at the micro-edge, such as artificial intelligence and signal and image processing. Multiplication is a crucial arithmetic process in such applications. However, large logic complexities typically seen in traditional multipliers generate combinatorial blocks with long chains of cascaded carry addition. As such, energy efficiency has remained a primary design challenge for these applications, when powered by batteries or emerging energy harvesters. Hardware multipliers are an essential component of signal processes and related algorithms embedded within numerous multimedia and communication systems. In Arithmetic Logic Unit (ALU) one-bit full adder is one of the most repeatedly used digital circuit component which is most integral functional unit of all computational circuit. In this paper CMOS CNFET, Memristor based full adder and Multiplexer circuits are implemented at 45nm, 180nm and 32nm technology and performance parameters such as Power Delay Product (PDP), Propagation Delay and Power Consumption are compared using Cadence Virtuoso, HSPICE and LTSPICE simulator software.

Keywords: CMOS, CNFET, Memristor Full Adder, Multiplexer, PDP.

INTRODUCTION

Today, pervasive electronic systems are integral part of everyday life. With the advancements in the technology, demand for usage of battery based portable systems or devices such as laptops, cellular phones, iPad, and IOT devices etc. is increasing day by day. Such applications need low power consumption, small area and high-speed operation. Arithmetic operations like addition, subtraction, multiplication and accumulation are the most common and widely used operations in many of the very large-scale integration and DSP architectures. 1-bit full adder is the basic building block used for

implementing these arithmetic operations. So, to enhance the performance of the overall systems, it is essential to enhance the performance of the basic full adder. Substantial performance progress improvement of the integrated circuits is due to endless scaling of the transistor size and decrease in operation voltage. Due to technology scaling to deep sub-micro level the speed of the circuit increases rapidly, but at the same time, due to increasing density of the chip, the power consumption increases. Therefore, in realizing modern VLSI circuits, power and high speed are the two principal parameters which need to be considered. Generally, a design trade-off is formed between propagation delay and power dissipation in full adders. If one is increase then the other is

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decrease. So, to analyze the performance of full adder in terms of delay and power, the product of power dissipation and propagation delay are used.

In this paper, full adder and Multiplexer is implemented with different design techniques i.e., fast full adder by using new XOR and XNOR gates (CMOS full adder), CNFET based full adder and memristor based full adder, CMOS based MUX and Memristor Based MUX and compare their performance parameters. The comparative analysis and simulations are done on power dissipation, propagation delay, area and power delay product (PDP) using cadence virtuoso tool in 45 nm and 180nm technology for CMOS based FA, HSPICE Software in 32nm technology is used for CNFET based FA while LT SPICE Software is used for memristor based FA circuit, CMOS and Memristor Based MUX.

RELATED WORK

Chandran Venkatesan, Thabsera Sultana M, SumithrabM.G and Suriya M [1] presented the comparison of different 1-bit full adder designs, namely 28T CMOS structure, 10T CMOS design 10T GDI (Gate Diffusion Input) design, 10T SERF (Static Energy Recovery Full Adder) design and 8T CMOS design [1]. Full adders with different logic styles (conventional, transmission gate, 14T, GDI) are implemented in [2][3][4]. First of all, in this paper, Yavar Safaei Mehrabani and Mohammad Eshgi proposed some two input xor/xnor circuits and then, they are employed to form novel 1-bit full adders [5] using CNFET technology. In this paper, Kawser Haghshenas, Mona Hashemi and Tooraj Nikoubin designed a two-energy efficient full address, in 32 nm CNFET technology. They use CDM logical style for design of proposed full address and CNFET-SEA, a new sizing algorithm is used for the device-circuit co-optimization [6][7]. In this paper Gongzhi Liu and his team proposes two kind of 4-bit carry look ahead adder based on hybrid CMOS- Memristor structure. One is based on MRL logic and other is improved one based on MRL universal gate [8]. while in [9] MAD gate is proposed which overcomes Scalability, applicability, completeness, and performance of memristor based gates. In [10] two-bit adder implemented based on memristor ternary logic gates (MTL) and verified by VTEAM memristor and CNTFET transistors.

In this paper Saeed Haghir and his team proposed Binary digital memristor based multiplier using IMP logic [11]. In [12] n bit modulo multipliers for (2^n-1) and 2^n radix is implemented using array multiplication. While [13] uses same method based on MRL logic. [14] [15] uses IMPLY logic style for implementing Memristor Multiplier. In [16] Shengqi Yu†, Ahmed Soltan and his team proposed mixed signal current mode multiplier using VTEAM model [17]. In [18] proposed two memristor-based implementations of an N-bit shift-and-add multiplier, one using IMPLY operations and a second using MAD operations.[19][20] design 4-bit Multiplexer using Memristor CMOS hybrid technology.

PROPOSED WORK AND IMPLEMENTATION

CMOS Based Full Adder

Hybrid FAs are made of two modules, including 2-input XOR/XNOR (or simultaneous XOR–XNOR) gate and 2-to-1 multiplexer (2-1-MUX) gate [21]. In the Full Adder cell XOR/XNOR gate is the extensive consumer of power. Therefore, the power consumption of the FA cell can be reduced by optimum designing of the XOR/XNOR gate. So, one way is to use a XOR/XNOR gate to reduce the power consumption of the Full Adder structures and a XOR or XNOR signal is generated by using NOT gate. The proposed hybrid FA cell (HFA-17T) shown in Figure 1 is designed to produce the output Sum signal, the XOR, XNOR, and C signals are only used so no additional NOT gates need to generate the C signal, whereas if the C signal is also used to produce the Sum output, then XOR and XNOR signals will not drive the Sum output through the TG multiplexer, but only they will be

connected to the data select lines of 2-1-MUX [21]. So, the capacitance of XOR and XNOR nodes become smaller and the delay of the circuit will be improved.

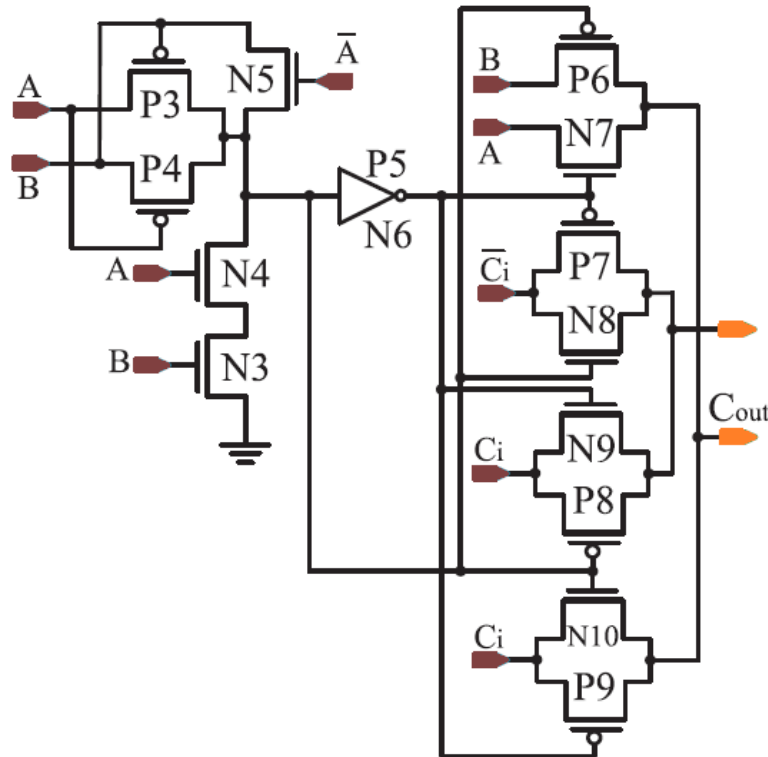


Figure 1. CMOS Based Full adder.

CNFET Based Full Adder

We have designed 1-bit full adder cells using carbon nanotubes field effect transistor in HSPICE. We have implemented this circuit in HSPICE using 32nm technology. This full adder cells provide good driving capability by decoupling input and outputs. This full adder employs PTL to provide XOR/XNOR function shown in Figure 2. This new pass transistor full adder (NEW-PT-FA) consists of 26 transistors. Critical path of the new full adder consists of 4 transistors. NOT gate is used at the output node then this structure provides good driving capability. When it is embedded inside large side in cascaded form then it guarantees the proper functionality. NEW-PT-FA cause leakage current and consequently large power consumption when non-swing outputs of XOR/XNOR embedded in it.

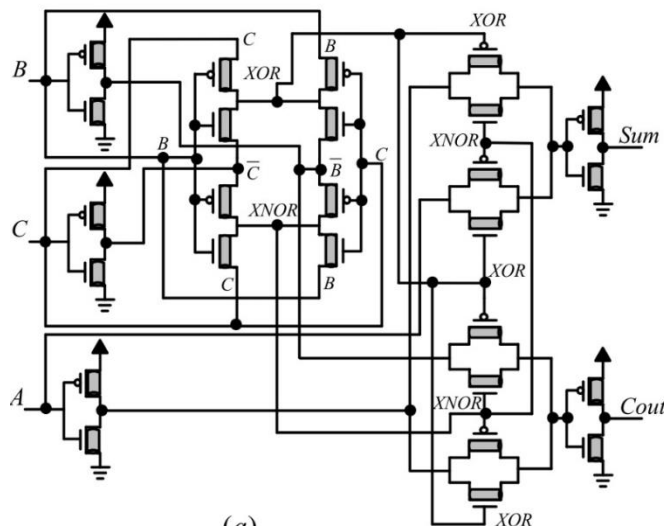


Figure 2. CNFET Based Full adder

Memristor Based Full Adder

Figure 3 shows universal Logic gate (ULG), which is combination of MRL logic and CMOS inverter. The universal logic gate (ULG) uses 4 memristors and 2 CMOSFET transistors to perform 3 logic functions at the same time: AND, OR and XOR. The main function of this circuit is that the output of logic AND gate is connected to the input of the inverter, the output of logic OR gate is connected to the source of the PMOS, and the output of logic OR gate is connected to the source of the PMOS, and the output of the inverter happens to form an XOR gate.

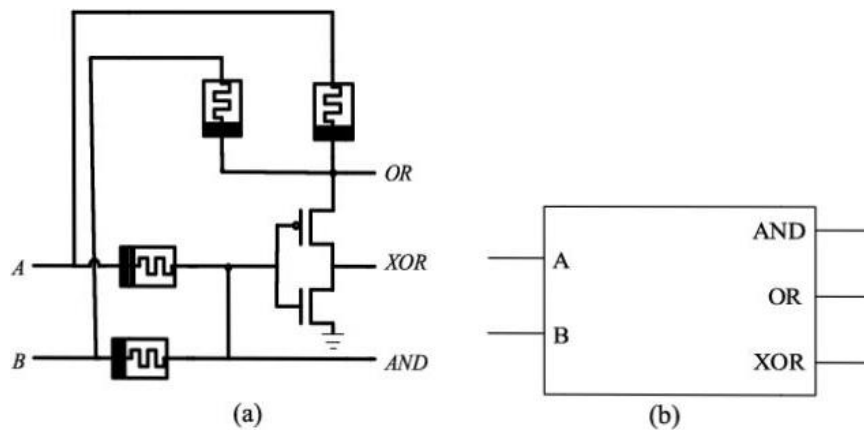


Figure 3. (a) ULG Circuit (b) ULG Symbol.

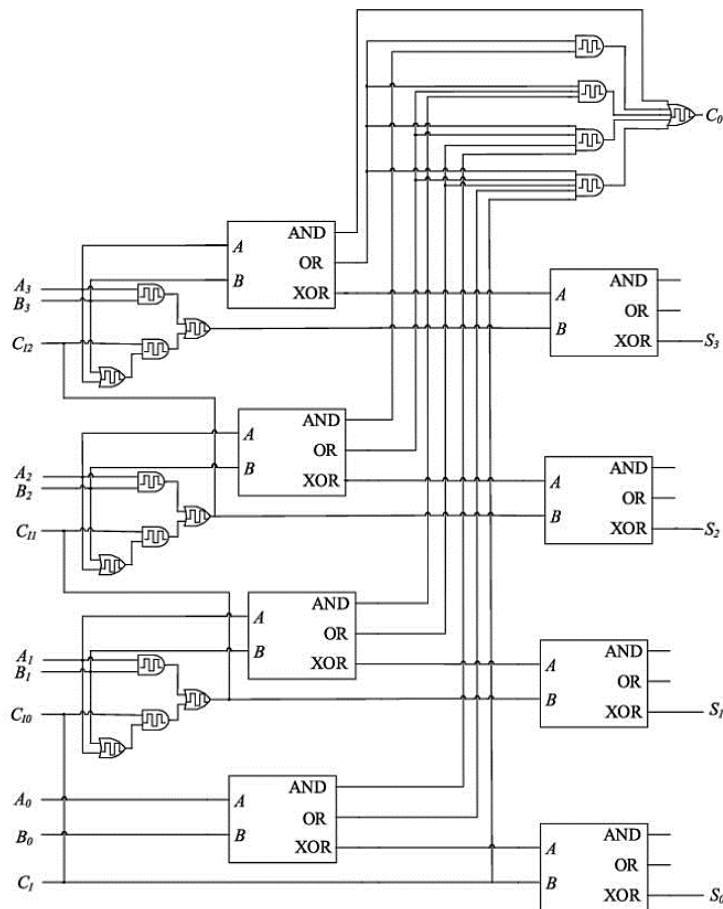


Figure 4. Improved carry-lookahead adder using Memristor.

Full Adder using Memristor shown in Figure 4 is implemented on LTSPICE Software at 32nm technology. This Full Adder is design using combination of ULG circuits and basic logic gates that are design using a Memristor.

CMOS Based Multiplexer

In static CMOS any logic design there is two parts pull up network and pull-down network. Pull up network is made by p MOS transistors and pull-down network is made by nMOS transistors. This design has P1, P2, P3, P4 as pull up network and N1, N2, N3, N4 as pull-down network [22]. Pull up network is connected to V_{dd} and pull down is connected to gnd. The complemented output is taken from A, shown in Figure. 5. The working of this circuit is explained as when

- $S=0, I_0=0, \bar{S}=1, I_1=1$ then P1 and P3 are ON, output A is high.
- $S=0, I_0=1, \bar{S}=1, I_1=0$ then N1 and N4 are ON, output A is low.
- $S=1, I_0=1, \bar{S}=0, I_1=0$ then P2 and P4 are ON, output A is high.
- $S=1, I_0=0, \bar{S}=0, I_1=1$ then N2 and N3 are ON, output A is low.

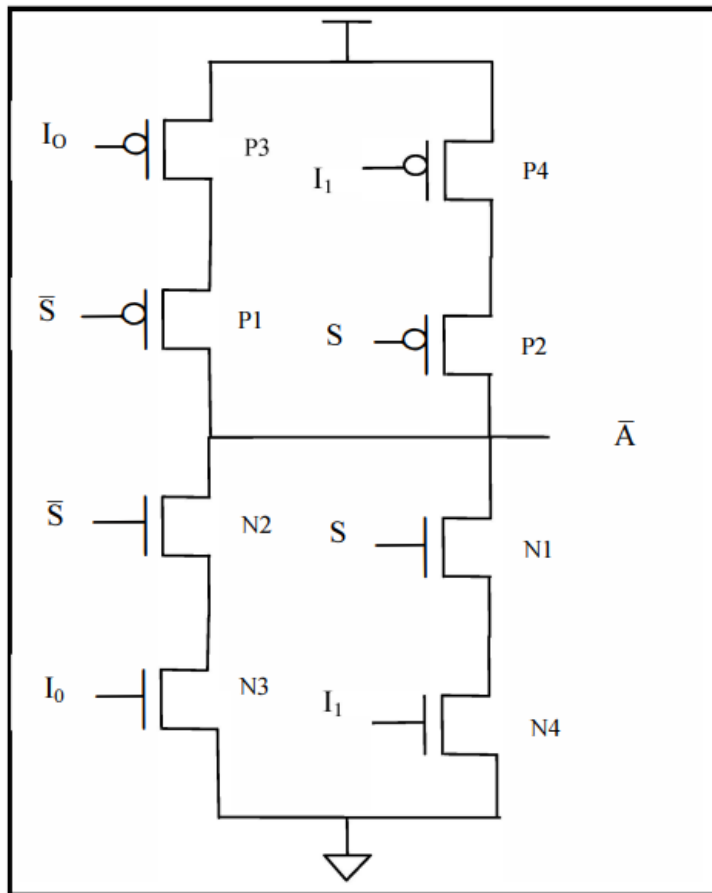


Figure 5. Schematic circuit diagram of static CMOS based 2: 1 Multiplexer

Memristor Based Multiplexer

It's based on resistance switching effects. In CMOS based design many transistors are used accordingly circuit complexity is increased. To reduce complexity Memristor is come in picture. To make multiplexer from Memristor four Memristors are used. In figure: M1, M2 are in one direction and M3, M4 are in opposite of them direction. Two nMOS transistors N1 and N2 are been used as pull-down network. One nano wire resistor is placed as pull up network. Selection line S is taken as vpluse and I_0 , I_1 are set to gnd and V_{dd} respectively. When S is low output will be I_0 and whenever S is high output showed the I_1 .



In this paper, CMOS based Full Adder is simulated on Cadence Virtuoso at 180nm and 45nm technology and CNFET based Full Adder circuit is simulated on HSPICE software at 32nm. Simulations for Memristor based FA, MUX and CMOS based MUX are conducted on a LT-HSPICE simulator using 32nm technology.

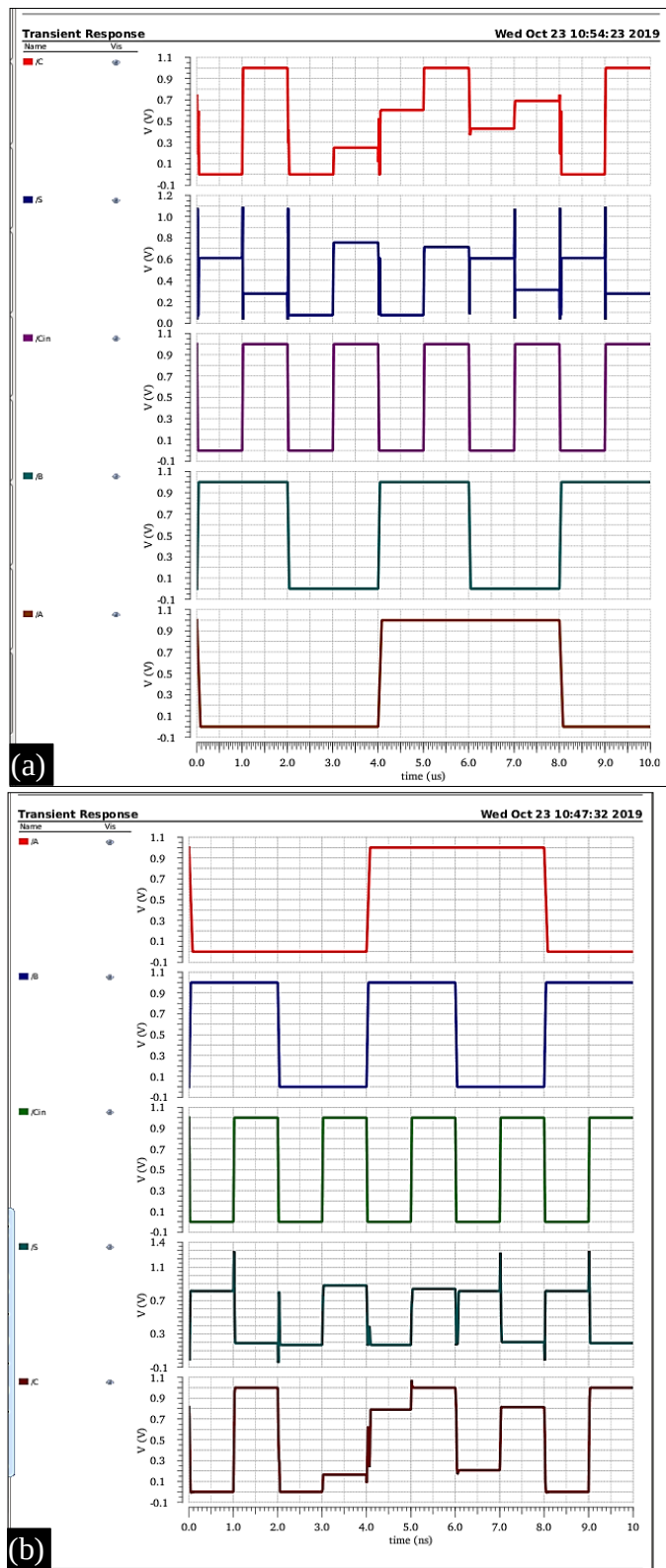


Figure 7. (a) Simulation output for proposed Hybrid. (b) Simulation output for proposed CMOS Full Adder at 180nm. CMOS Full Adder at 45nm

Simulations for CNFET based FA are conducted on a HSPICE simulator using 32nm technology.

Figure 8 shows the circuit of proposed full adder and power & delay analysis for the same is also given below.

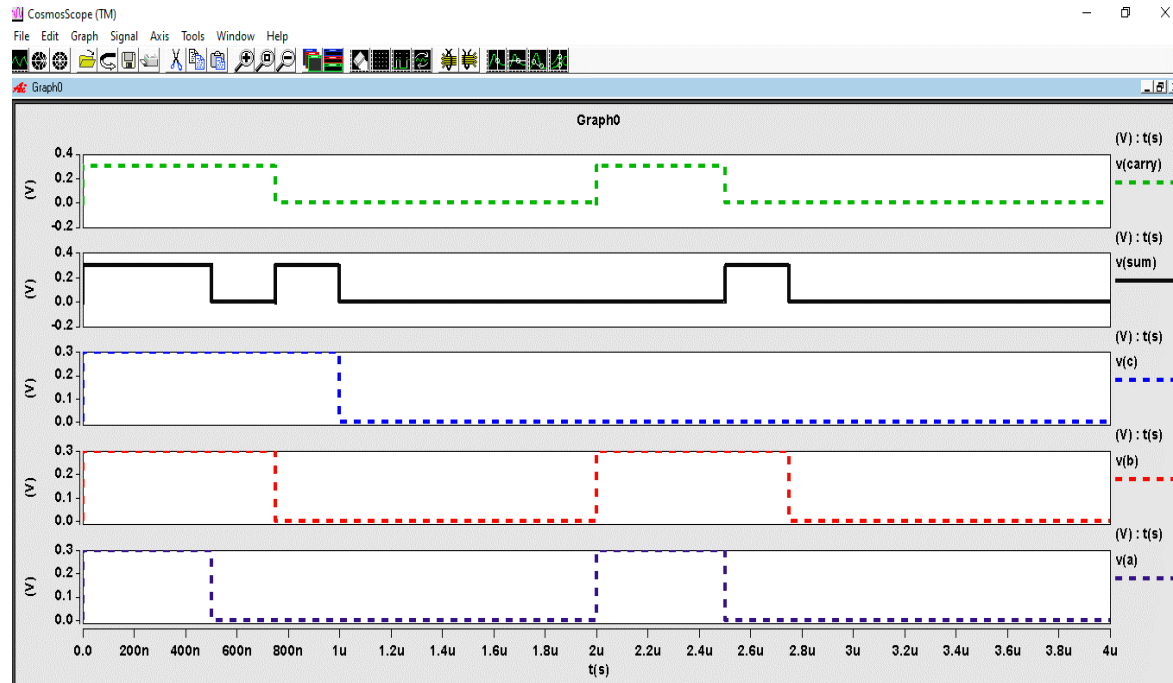


Figure 8. Simulation output for proposed Hybrid CNFET Full Adder at 32nm.

Simulations for Memristor based FA are conducted on a LT-HSPICE simulator using 32nm technology.

Memristor based FA is implemented on LTSPICE shown in Figure 4 & Its input output waveform shown in Figure 9 Waveform satisfy the truth table of FA. Hence the circuit is correctly working as a FA circuit.

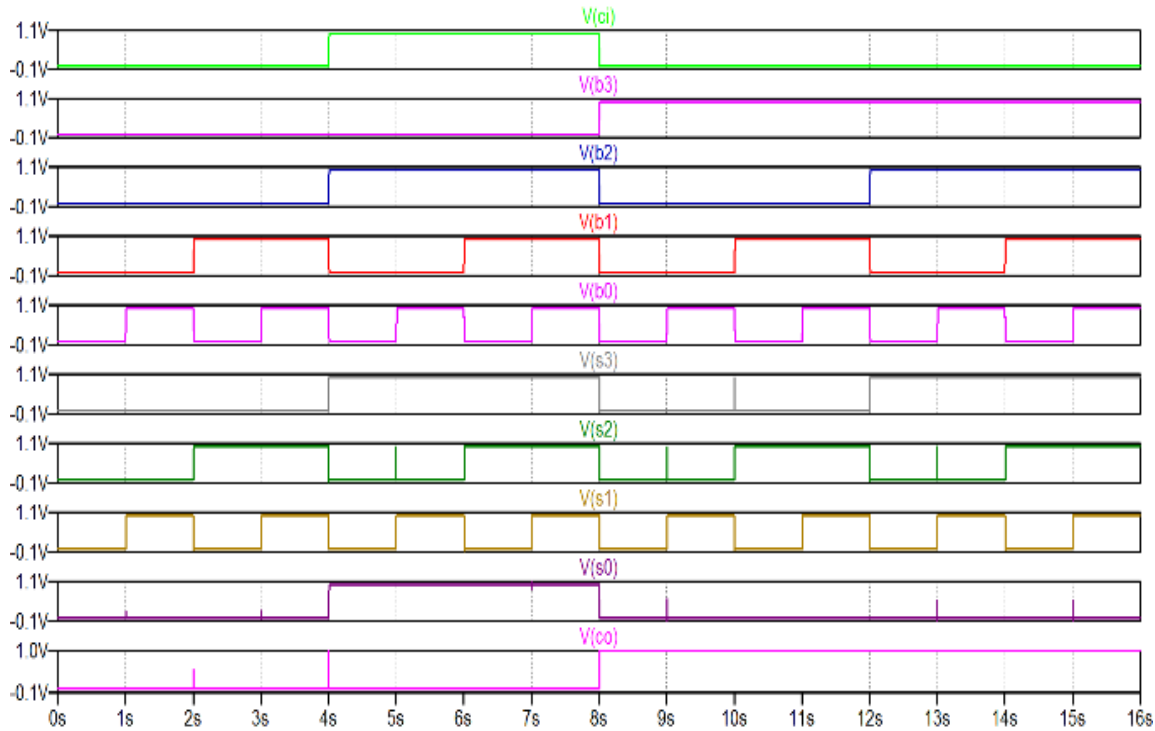


Figure 9. Simulation output for proposed Memristor Based Full Adder at 32nm.

Table 1. Simulation Result of Proposed Full Adder.

Technology	Design	Propagation Delay	Avg. Power Dissipation	Power Delay Product
180nm	Hybrid CMOS FA	5.005×10^{-9}	67.58×10^{-6}	33.8×10^{-14}
45nm	Hybrid CMOS FA	3.655×10^{-9}	3.788×10^{-6}	1.38×10^{-14}
32nm	Hybrid CNFET FA	104.16×10^{-9}	0.363×10^{-9}	3.47×10^{-17}
32nm	Memristor Based FA	-	-	1.14×10^{-17}

Table 1 shows the improvement in PDP as the technology reduces from 180nm to 32nm and also by using different transistors.

PDP of Memristor based FA is 1.14×10^{-17} which is very less as compared to CNFET and CMOS based FA circuit.

CMOS based 2:1 Multiplexer is implemented on LTSPICE shown in Figure 5 & Its input output waveform shown in Figure 10 Waveform satisfy the truth table of 2:1 MUX. Hence the circuit is correctly working as a 2:1 MUX circuit.

Memristor based 2:1 Multiplexer is implemented on LTSPICE shown in Figure 6 & Its input output waveform shown in Figure 11 Waveform satisfy the truth table of 2:1 MUX. Hence the circuit is correctly working as a 2:1 MUX circuit.

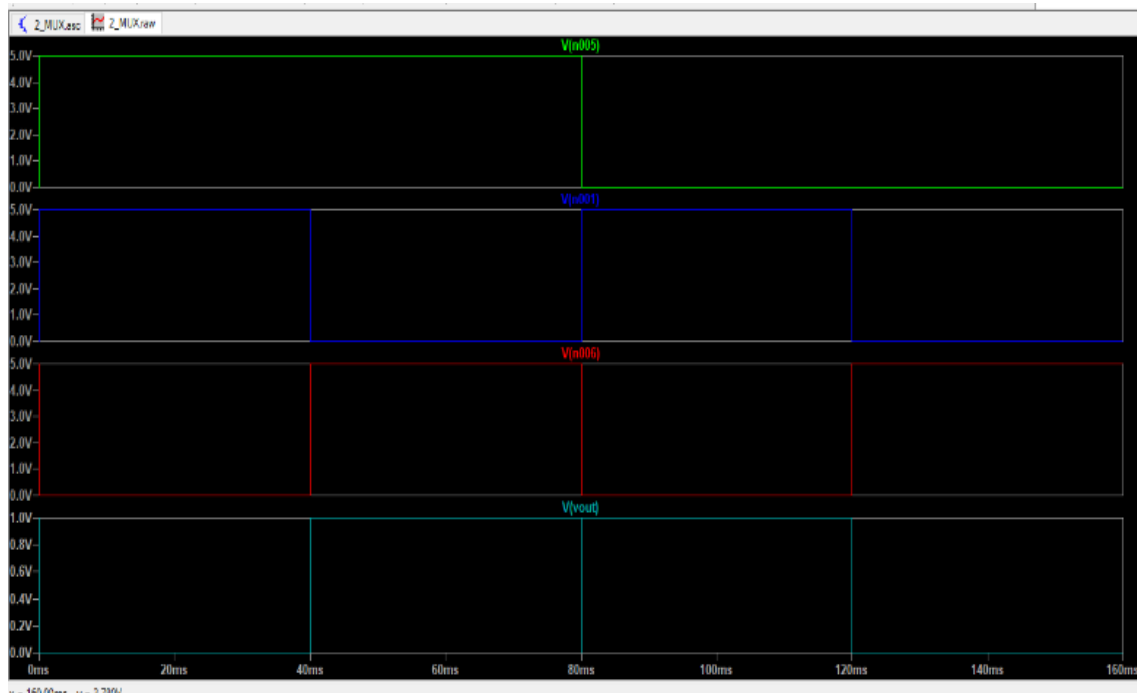


Figure 10. Simulation output for CMOS based 2:1 Multiplexer.

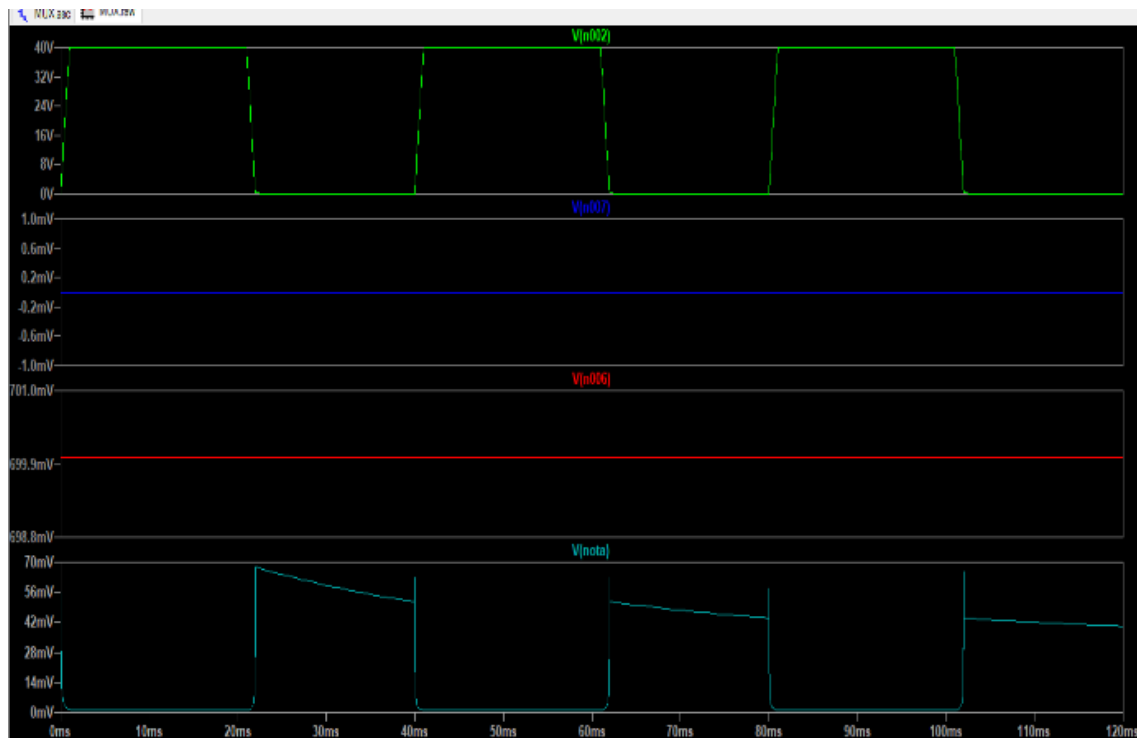


Figure 11. Simulation output for Memristor based 2:1 Multiplexer

Table 2. Simulation Result of Proposed Multiplexer.

Technology	Design	Propagation Delay	Avg. Power Dissipation	Power Delay Product
180nm	CMOS Based 2:1 Multiplexer	3.21×10^{-9}	6.9×10^{-6}	2.214×10^{-12}

32nm	Memristor Based Multiplexer	2:1	2.357×10^{-9}	5.45×10^{-6}	1.28×10^{-14}
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CONCLUSION

In this paper, we first evaluated the CMOS based Full Adder circuits using CADANCE VIRTUOSO software at both 180nm and 45nm technologies. The evaluation revealed that the Full Adder circuit at 180nm technology has larger PDP i.e., 33.823×10^{-14} joules as compared to 45nm technology Full Adder i.e., 1.3845×10^{-14} joules. We proposed CNFET based Full Adder circuit which is simulated using HSPICE software at 32nm technology. The simulation results demonstrated that the proposed CNFET based Full Adder circuit has superior speed and smaller PDP (3.4735×10^{-17}) as compared to CMOS based Full Adder circuit. The proposed memristor based Full Adder circuit is simulated using LT-SPICE software at 32nm technology. Simulation results show that the proposed carry look ahead Full Adder having very a smaller number of memristors and CMOSs significantly has very less power consumption and chip area. Similarly, simulation result of CMOS based Multiplexer and Memristor based Multiplexer done on LT-SPICE and its simulation shows that proposed Memristor based MUX has superior speed and smaller PDP as compared to CMOS based MUX.

The comparative analysis of all the performance parameters i.e., propagation delay, power dissipation and PDP of all the three full adder and Multiplexer circuits shows that the memristor based Full Adder and Multiplexer circuit has very good performance over both CMOS and CNFET based Full Adder and Multiplexer circuits.

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