

Design and Simulation of LNA in 90 nm CMOS Technology for Radio Receiver using the Cadence Simulation Tool

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Abstract

Due to its successful operation in the 2.4 GHz frequency region, often known as the ISM (Industrial, Scientific, and Medical) band, RFICs play a vital role in communication systems. The major parts being used transceivers for frequency translation and amplification are LNA and Mixers. Different types of mixers and LNAs are employed, and different strategies are used to optimize them. In this paper an approach for design and simulation of cascode LNA is discussed to increase to efficiency and Radio Frequency (RF) performance of LNA. More emphasis is put here on the optimization of design. The LNA parameters show how the amplifier is going to work for the proposed design. A low noise amplifier simulated in 90 nm CMOS technology. The proposed cascode LNA consists of two transistors. It exhibits 2.5-dB noise figure and 23-dB gain at 2.4 GHz while consuming only 44 nW, this results are confirmed after post layout simulations. These straightforward and analytical conclusions are particularly important since they may be used not only to build CMOS LNA circuits, and to characterise and diagnose them, whether functional prototypes or built. The Communication System's core building block or key component is a Low Noise Amplifier. Any radio receiver is made up of a Low Noise Amplifier, a mixer, and a Filter (Power Efficient Active Filter), with the LNA playing a critical part in the circuit as an amplifier.

Keywords: Cascode low noise amplifier, LNA designing for 2.4 GHz, LNA simulation, Cadence Virtuoso simulation of LNA.

INTRODUCTION

With speedy development of communication business, additional and additional types of wireless communication modules square measure required, such as tiny power radiation, way effective distance, huge coverage vary, have been the main target of the bourgeois and the manufacturer of the wireless communication modules. In this condition, swift organic process radio frequency (RF) wireless communication technology has been widely utilized in all fields of the planet. Low noise electronic equipment (LNA) that is within the RF front-end circuit has the nice worth during this field. The LNA comes in the early stage of a receiver, its function is to provide gain to compensate for the noise for the subsequent stages. The LNA should add noise as minimum as possible and can contain large signals without any kind of distortion, and for maximum power transfer there should present a specific impedance ($50\ \Omega$) to the source impedance. In present times,

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the LNAs are very crucial. LNAs are found in communication systems, such as in radio communication, in various Bio-medical instruments and various other electronic equipment.

The initial stage of a receiver is generally a low-noise electronic equipment (LNA), whose main performance is to give enough gain to overcome noise of resultant stages (for example, in the mixer or IF amplifier). Aside from providing enough gain, whereas adding as very little noise as attainable, associate degree LNA ought to accommodate massive signals while not distortion, supply a massive dynamic vary, and gift smart matching to its input and output, that is extraordinarily necessary if a passive band choose filter and image-reject filter precedes and succeeds the LNA, since transfer characteristics of the many filters are quite sensitive to the standard of the termination. The following diagram Figure 1 shows the position of a LNA in a communication system. The RF receiver architecture consists of a RF Filter, LNA, Image filter, Mixer and Local Oscillator (LO).

The usual LNA sometimes have a good gain value but very poor noise figure or vice versa. So for a quality LNA both values should be nearly ideally matched to the designed value. Hence, I proposed the LNA having good value for gain as well as for noise figure and other parameters like reverse isolation too. In [1], the proposed LNA in this paper is for 2.4 GHz wireless applications. This paper describes the design of a single-ended CMOS LNA with gain boosting and improved linearity. With the feed forward technique, this design consumes 2.6 mW of power while producing an IIP3 of -5.18 dBm and a noise figure of 4.2 dB. The author in [2] designed and simulated LNA in 45 nm CMOS process and it get a low input reflection coefficient (S_{11} -15 dB) and high linearity LNA using cascode with inductively degenerated topology is reported in this paper. At 2.4 GHz, the proposed LNA achieves IIP3 of 14.097 dBm, S_{11} of -22.627 dB, reverse transmission coefficient (S_{12}) of -39.539 dB, and moderate gain of 18.390 dB. In [3], author discussed about discusses the differential input differential output low power high gain LNA For 2.4 GHz applications using TSMC 180 nm CMOS process where the propose LNA displays very high gain with a very low noise figure and at 2.4 GHz frequency it is highly linear and stable.

DESIGN METHODOLOGY

The designing of low noise amplifiers considers many parameters such as, minimizing noise figure of amplifiers, providing high gain with ample one-dimensionality, and supporting stable input and output impedance. The typical characteristics of a LNA are having gain something between 10–20 dB, Noise Figure (NF) should be as minimum as possible (<3 dB typically), reverse isolation should be as high as possible [4–6].

Although common source LNA is one of the most used topology for designing the LNA, but it has some serious disadvantages. This disadvantage includes poor reverse isolation due to Cgd. The Cgd further affects the stability due to presence of zero in transfer function. These disadvantages can be understood from Figure 2.

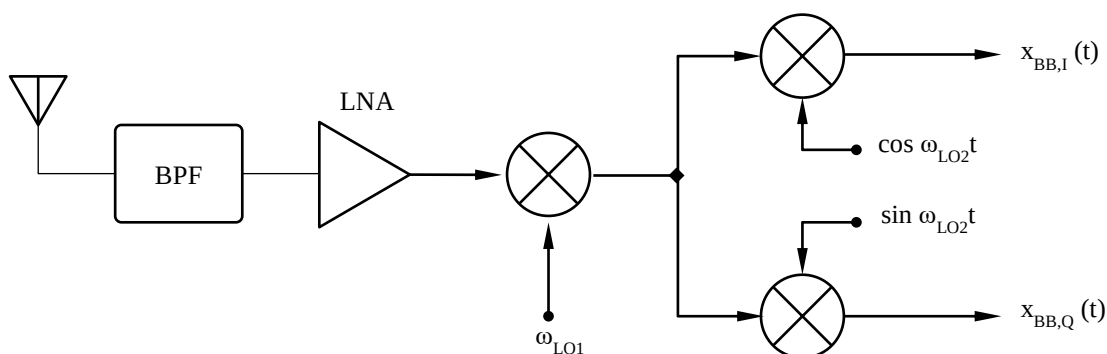


Figure 1. LNA in a communication system.

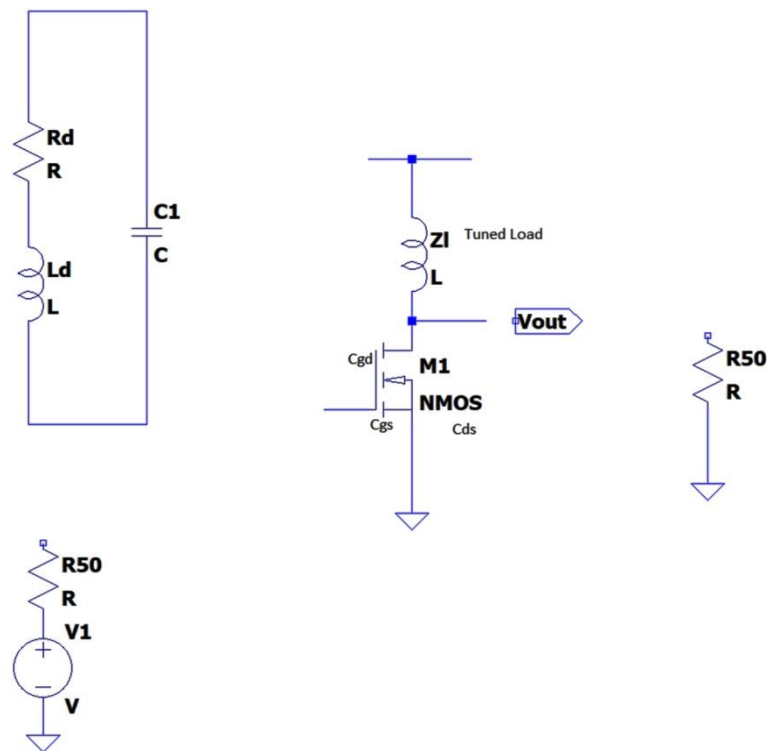


Figure 2. Common source LNA

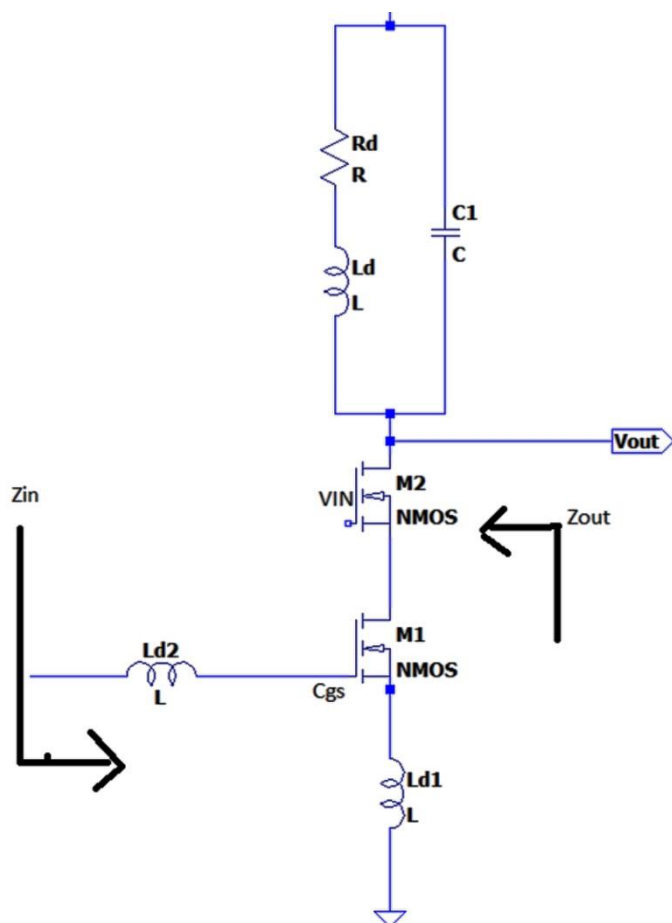


Figure 3. Cascode source degeneration common source topology for LN.

Thus the remedy for these is a cascode source degeneration common source which also is popular LNA design topology. The cascode improves input-output isolation (or reverse isolation) as there is no direct coupling from output to input. Which eliminates the Miller effect and so contributes to a way bandwidth measure. However, cascode LNA should have a higher provided voltage since voltage should be shared. Also, there is a reduced signal swing that will have an effect on the linearity or the one-dimensionality of the circuit. The cascode source degeneration common source topology for LNA can be illustrated by Figure 3. Here it consists of two transistor structure. The lower part or the common source stage is known as the amplifying transistor (M1) and the above part or the common gate stage is the cascode transistor (M2). For the gate of M2 which is ac ground so the output cap. Due to Z_{out} it is C_{gd2} only. The impedance looking to source of M2 is $1/gm^2$ as a result the miller effect is decreased [7–8].

PROPOSED LNA DESIGN

The architecture of the designed cascode low noise amplifier is shown in Figure 4. M1 is amplifying transistor and M2 is cascode transistor. The design is with a matching network which gives matching for 50 ohms. The input matching network can be designed by passive components. First after determining the C_{gs} and g_m value we can find the value of L_g . The value of L_s can be around 0.2–0.26 nH. Now similarly we have to match for the output side using L_d and C_d out of which one component will be known and other can be found out by using following equation:

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (1)$$

For designing a LNA following design considerations were made:

- *Gain*: ~ 20 dB
- *Noise Figure*: < 3 dB
- *Input/output impedance*: 50 ohm
- *Reverse Isolation*: > 40 dB

There would be three stages in designing the LNA:

1. Input Matching
2. LNA Biasing
3. Output matching

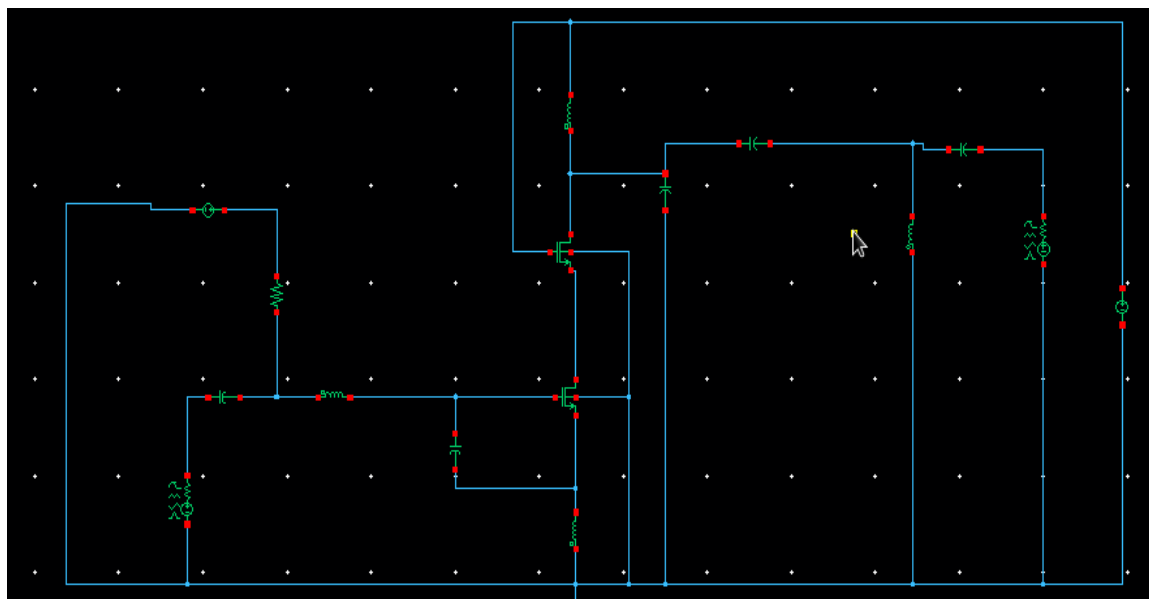


Figure 4. Proposed LNA.

Prior to this we have to find certain values that will be needed for determining the further parameters. We need the value of V_{th} , μ_n and t_{ox} which can be determined by DC analysis and we assume a Power Dissipation (PD) = 2 mW, from which we will be getting $I_D = 2$ mA (Considering $V_{DD} = 1$ V). Next step will be getting the values of oxide capacitance (C_{ox}) and trans conductance (gm). For input matching, the value of input resistance R_s value for LNA is 50 ohm. The value of source inductor for the amplifying transistor $L_s = 0.2$ nH, it should be in range of 0.2–0.26 nH. We need a gate-source capacitance [C_{gs} (external)] that will be needed to connect with LNA to compensate for the parasitic capacitance associated with transistor C_{gs} (MOS). Following which we finally find the value of gate inductance (C_{gs}). A bias voltage is given by connecting a dc bias along with a large valued resistor. This bias is applied to the gate terminal of the input transistor. For final stage i.e. output matching, we have the load inductor and capacitor, out of which one value is known to us and the other can be determined by using the equation, $f = 1/(2\pi\sqrt{L_d * C_d})$, (where f is our targeted frequency for which the LNA is designed). The final design of the LNA can be seen in Figure 4.

RESULTS AND DISCUSSION

To check the performance of the proposed LNA, certain analysis like AC analysis, Noise analysis, Transient analysis, S-parameter analysis, 1-dB compression point.

AC analysis

Ac analysis is used to figure out the Frequency Response of the circuit. It is used to measure the circuit bandwidth, low cutoff frequency, the gain, Phase angle, Q-factor, dissipation factor, maximum and minimum impedance. From the 20 dB graph, gain value is received as 23 dB at 2.4 GHz as shown in Figure 5.

Noise Analysis

Noise analysis is carried for calculating the noise at output side to the noise at input. The value of Noise Figure (NF) can be found out as 2.16 dB at 2.4 GHz which is less than 3 dB shown in Figure 6.

Transient Analysis

Transient analysis gives a clue on how a circuit behaves changes in the driving voltage/current. Genuine circuit reaction to changes in the driving voltage can be difficult to anticipate because of capacitance and inductance inside the circuit. The output waveform of the LNA can be visualized by this analysis. We can notice that the signal is not coming properly until around 20 ns time as shown in Figure 7.

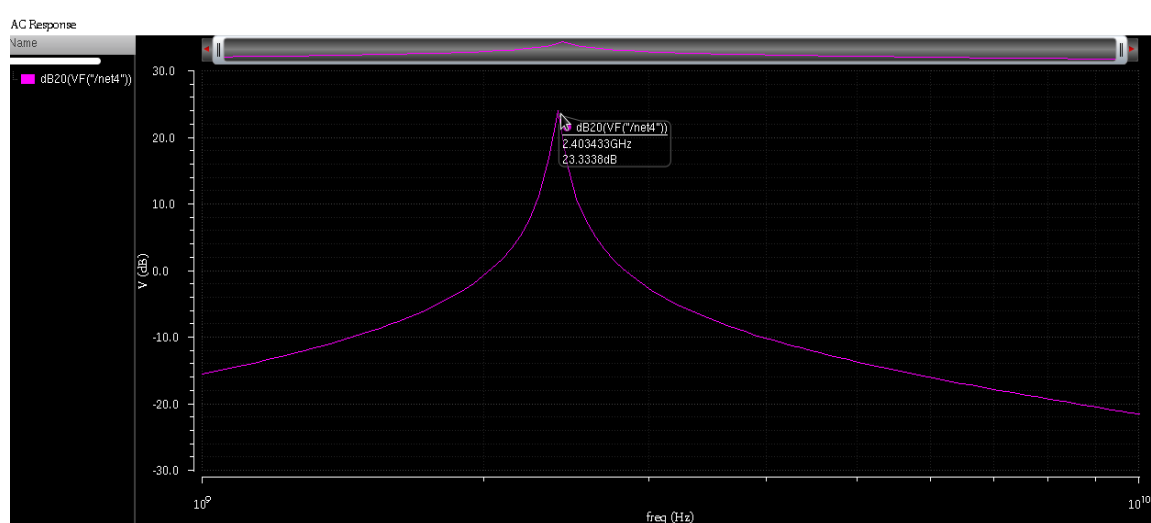


Figure 5. AC analysis of proposed LNA.

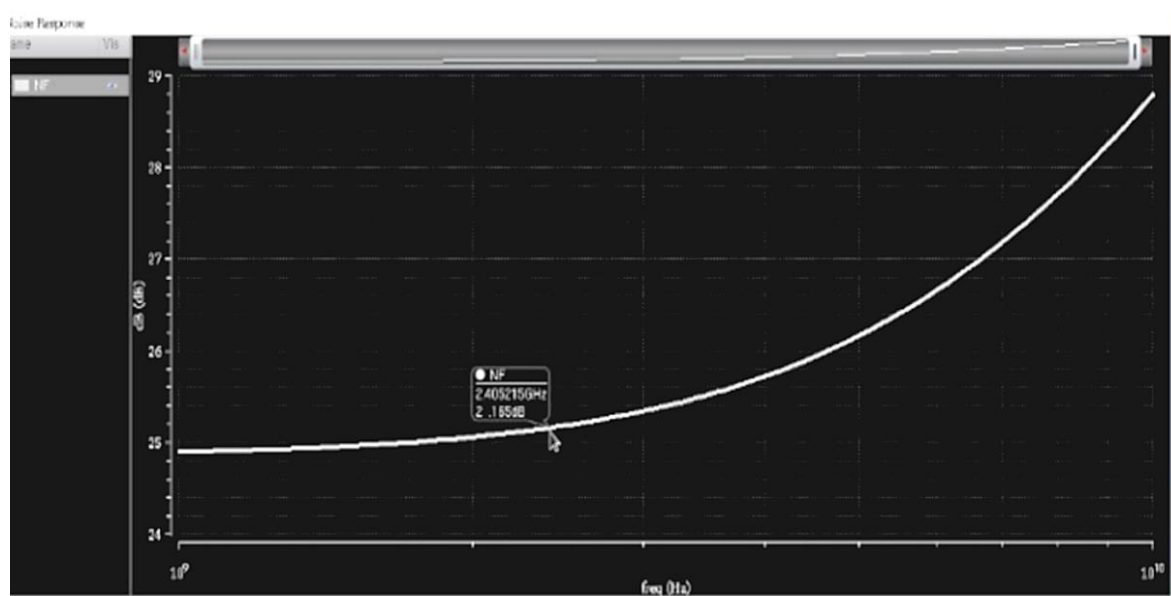


Figure 6. Noise analysis of proposed LNA.

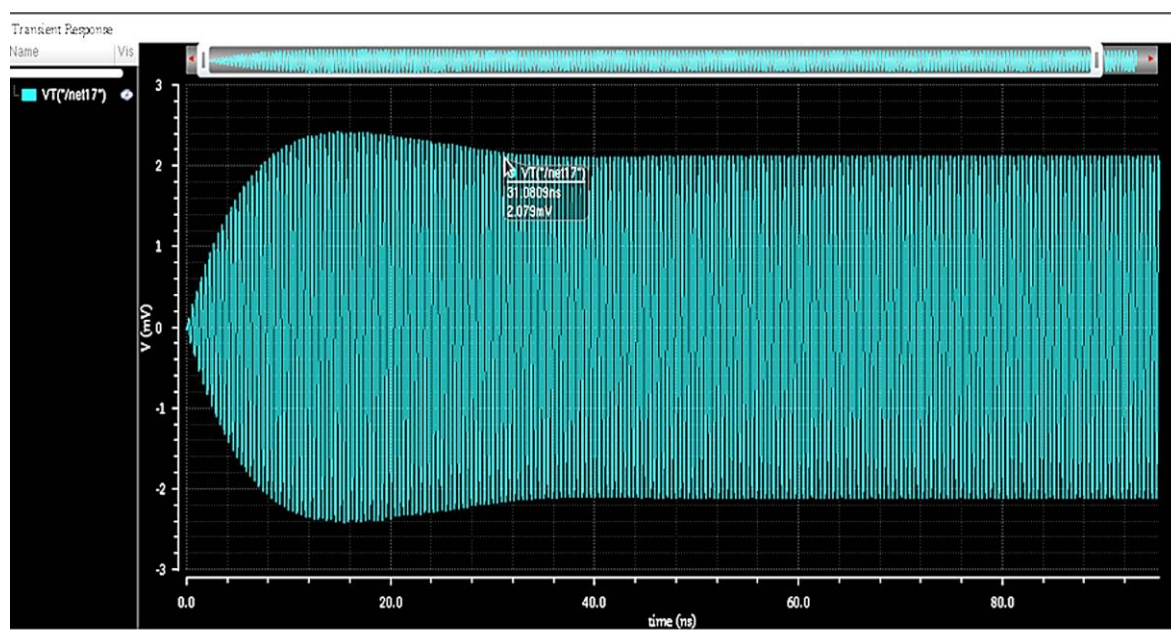


Figure 7. Transient analysis of proposed LNA.

S-parameter Analysis

The Scattering parameter/S-parameter gives us various information about the LNA such as the, S11 and S22 gives us the input/output port matching parameter respectively shown in Figures 8 and 9, S21 gives us the forward voltage gain and S12 gives the value for reverse isolation which is shown in Figures 10 and 11 respectively. All these parameters analysis can be observed in below simulation results.

1-dB Compression Point Analysis

From 1-dB compression point analysis, the understanding of the output power from where gain starts decreasing at value of 1 dB from its constant value [9–11]. Understanding like from which point distortion is produced and device become non-linear can be done by 1-dB compression point analysis. For the proposed LNA, Figure 12 shows the graph of 1-dB compression point which is at -16.1 dBm.

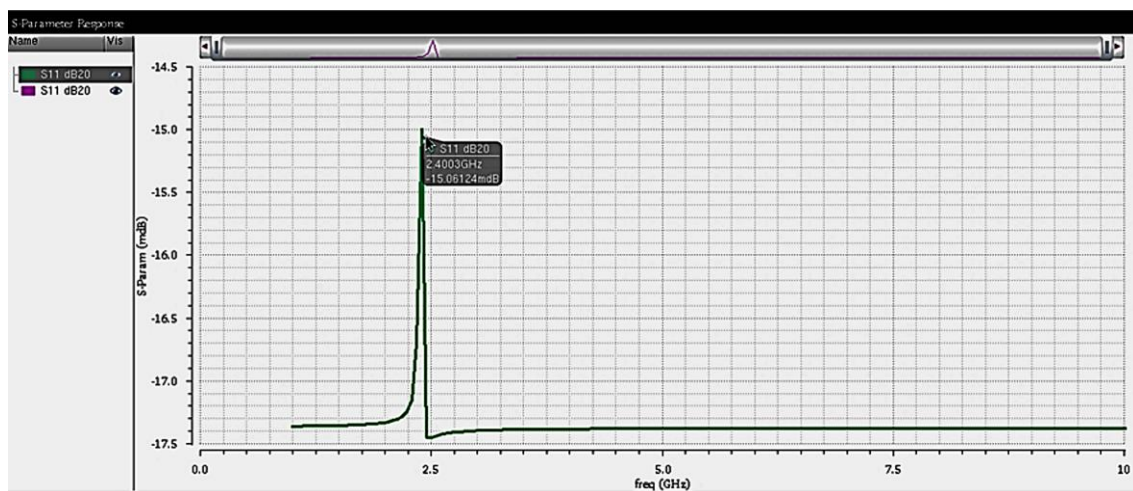


Figure 8. S11 analysis of proposed LNA.

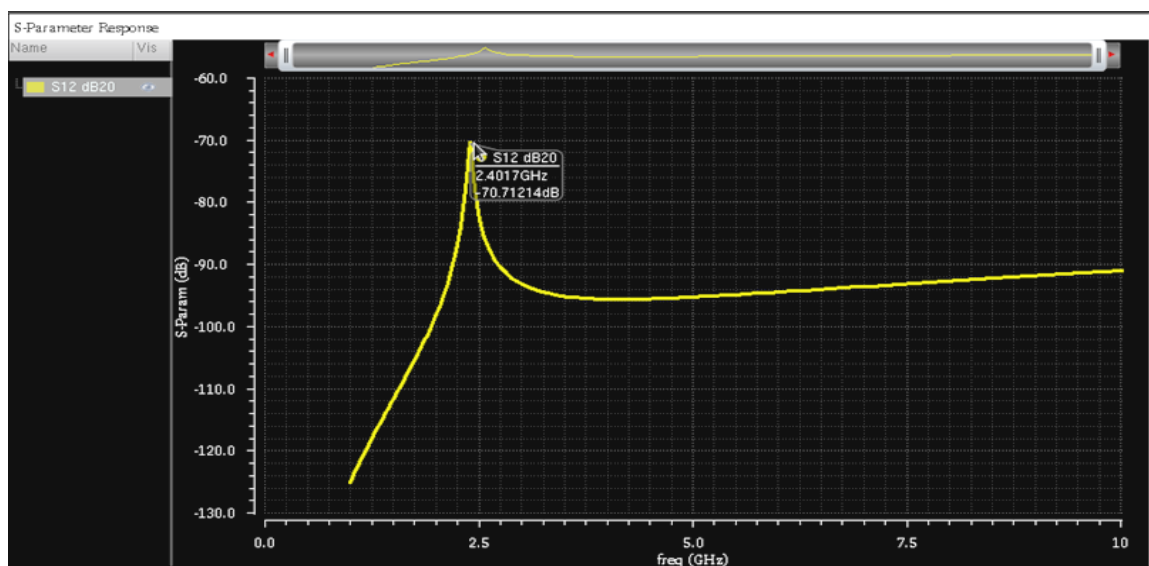


Figure 9. S12 analysis of proposed LNA.

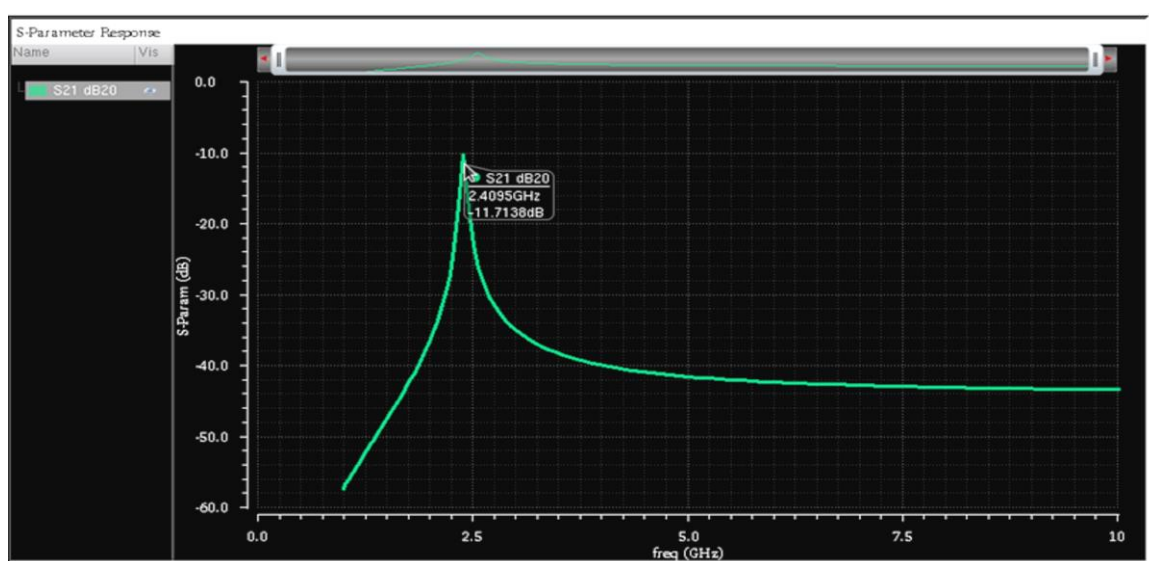


Figure 10. S21 analysis of proposed LNA.

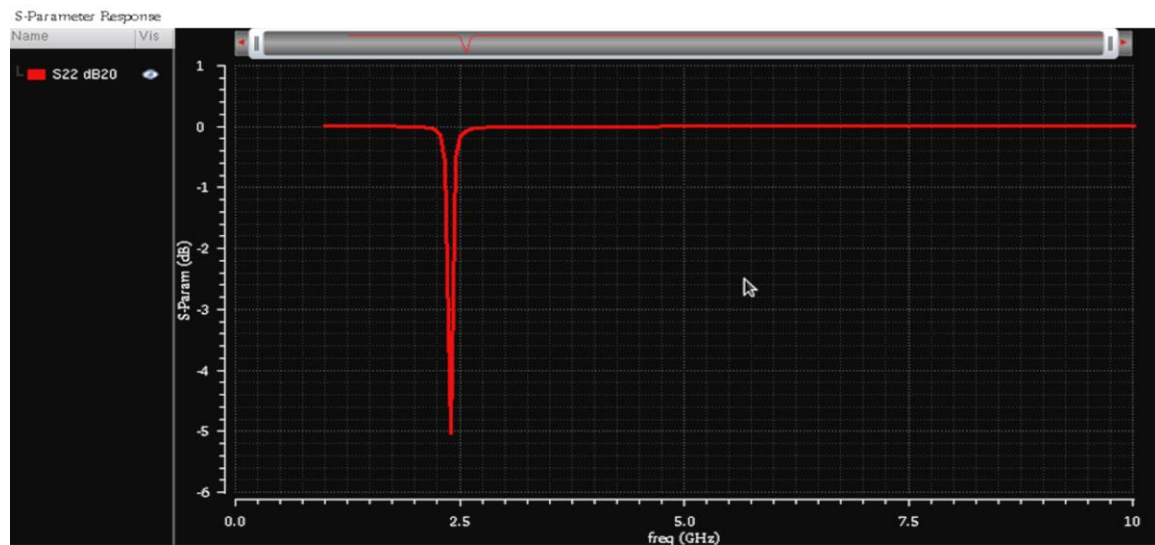


Figure 11. S22 analysis of proposed LNA.

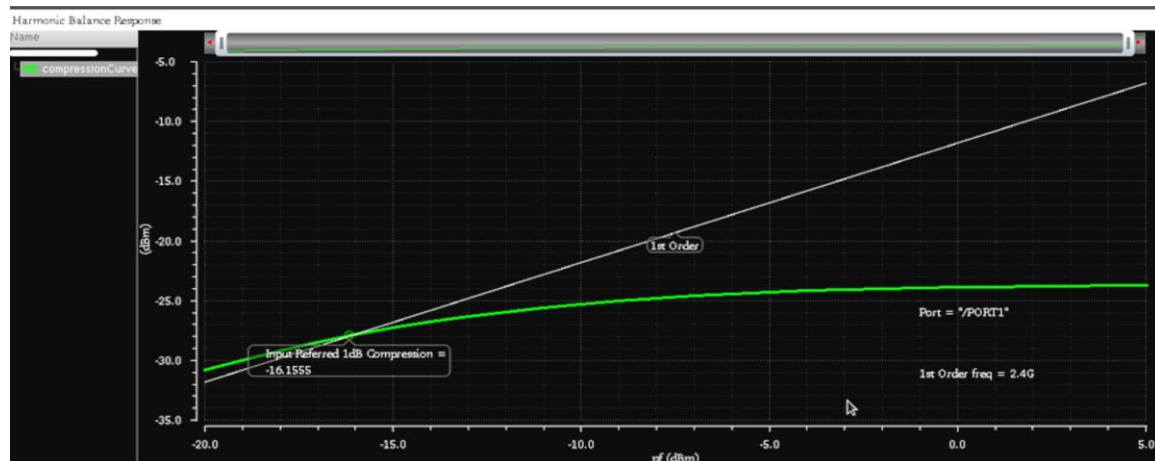


Figure 12. 1-dB compression point analysis of proposed LNA.

CONCLUSION

The research work resulted in the design of a new Low Noise Amplifier (LNA) circuit for frequency 2.4 GHz, as well as circuit simulation in Cadence ADE (L). The simulation findings are very similar to the post-layout outcomes. As described in the simulation section, the suggested LNA has a high gain and a very less value of noise figure. The LNA is better suited for RF Radio Receiver circuits because it can perform and work with a wide range of Noise Amplifiers. The increased FOM suggests that the proposed LNA architecture could be a good fit for low-cost, high-speed wireless applications. The comparison Table 1 shows that the proposed LNA achieves a large bandwidth, improved gain, reduced chip area, and low NF without affecting other LNA FOMs.

Table 1. Comparison of the proposed LNA with state-of-the-art LNAs.

Ref	[8]	[9]	This work
Tech.	180 nm	180 nm	90 nm
Gain (dB)	9.3	12.4	11.71
NF, dB	4–8	4.4–6.5	2.15
BW, GHz	2.3–9.2	0.4–10	2.4
S11, dB	<-9.9	<-10	<-15.06
S12, dB	—	—	<-70.71
IIP3, dBm	-6.7	-6	-16.15

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